NETWORK of EXCELLENCE
DESIGN FOR MICRO & NANO MANUFACTURE PATENT (DfMM)

DfMM NoE PATENT

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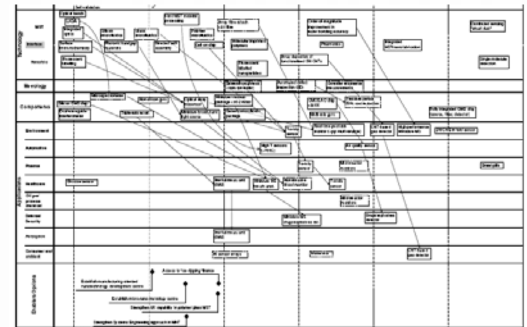
Technology Roadmapping: Packaging of MEMS

Objectives

- Using internationally recognized Technology Roadmapping techniques (Sandia Labs, Institute of Management of Cambridge) in 2 dedicated workshops to identify a common packaging vision for industrialists and academics.
- Gain a better understanding of growth opportunities, industry requirements and key gaps and barriers in packaging to the development of microsystems.
- Use the results of the Roadmap to target DfMM investments

Partners involved and roles

- HWU, UK (Project management, roadmapping process, organisation of workshops)
- QinetiQ, UK (Roadmapping process, organisation of workshops)
- Fraunhofer IZM, Germany (workshop organisation)



Summary of results

- Literature survey and reports on existing roadmaps
- Focus of 2 roadmapping workshops agreed
- 1st workshop delivered at HWU on 16/02/06, Gathering 30 academics, SMEs and large companies, More than half from industry

Table 4: Packaging Challenges through 2007

Difficult Challenges (Through 2007)	Summary of Issues
Improved organic substrates	Tg (Glass Transition Temp.) compatible with lead-free solder processing
	Increased wireability at low cost, substrates are a barrier to flip chip adoption
	Improved impedance control and lower dielectric loss to support higher frequency applications
	Improved planarity and low warpage at higher process temperatures
	Low moisture absorption
	Low-cost embedded passives
Improved underfills for flip chip on organic substrates	Improve flow, fast dispense/cure, better interface adhesion, lower moisture absorption
	Higher operating range for automotive and Pb free soldering in liquid dispense underfills
	Improved adhesion, small filler size, and improved flow for mold based underfills
Coordinated design tools & simulators to address chip, package, and substrate co-design	Chip, package, and system level co-design tools
	Educational programs required to train engineers in co-design technologies
	Faster analysis tools for integrated thermal mechanical analysis
	Higher accuracy, faster electrical simulation capability for high frequency design
Impact of Cu/low κ (dielectric constant) on packaging	Direct wirebond and bump to Cu (Copper)
	Bump & underfill technology to assure low κ dielectric integrity
	Improved Mechanical strength of dielectrics
	Interfacial adhesion
Pb (lead), Sb (antimony), and Halogen free packaging material	Lower cost materials and processes to meet new requirements, including higher reflow temperatures.
Difficult Challenges (Beyond 2007)	
Package cost which may greatly exceed die cost	Reliability under thermal cycling (stress and moisture)
	Research investments required for packaging cost reduction are decreasing
Small, high pad count	Array I/O pitches below 80 microns
High Frequency die	Substrate wiring density to support >20 lines/mm
	Lower loss dielectrics
	Skin effect above 10Ghz

Offer to industry

- A packaging vision and roadmap

Contact

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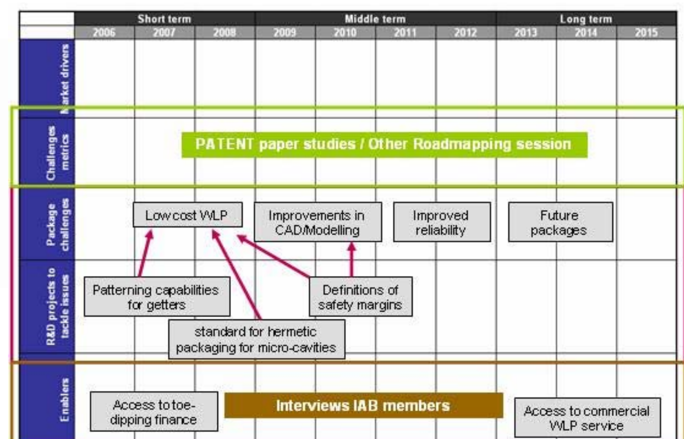

Project status, date:

Second workshop and final report are planned for May/June 2006

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