



Technology Roadmapping : Packaging of MOEMS and RF MEMS

16 February 2006

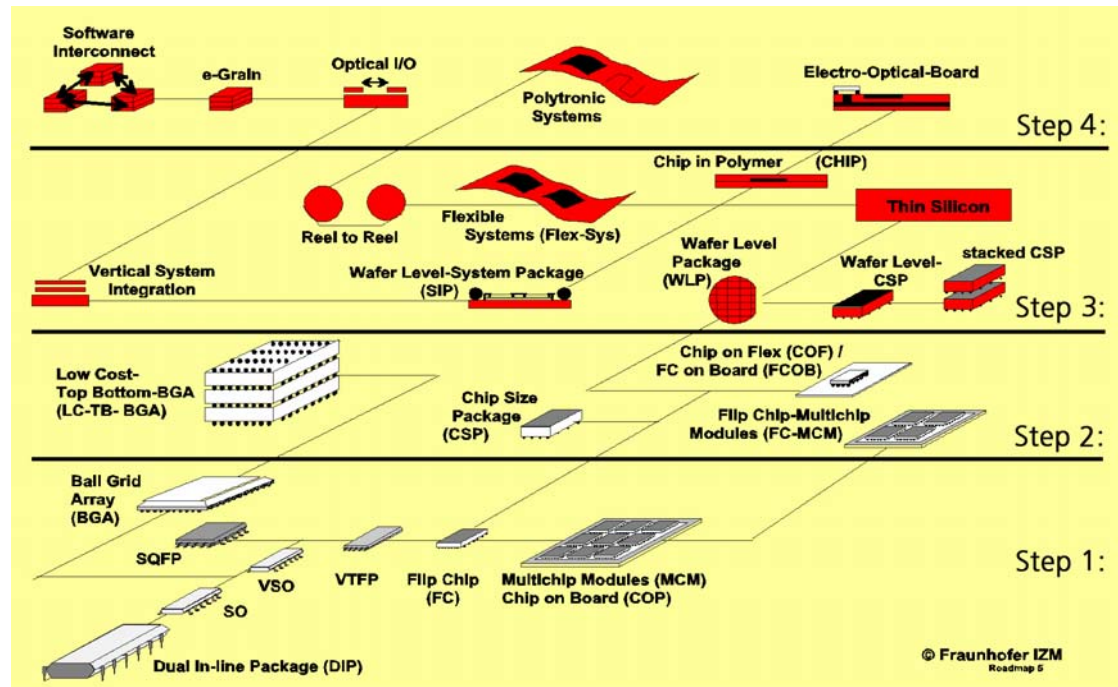
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Mar-06

- Technology Roadmapping is a process by which the timescale for future technologies and capabilities may be presented in a diagrammatic or tabular format to describe a future vision.
- When read in conjunction with the requirements of a particular organisation, the roadmap helps to identify technologies and capabilities that are critical to realising a future vision.

Today we are going to concentrate on capturing information to populate our technology roadmap on MOEMS and RF MEMS

- Existing relevant roadmaps: IZM, ITRS, NEXUS, MANCEF, MEMSTAND and various others from the internet
 - There are few elements of technology roadmap for packaging of MEMS
 - But, some very good table formats to be used in our project



Source: IZM

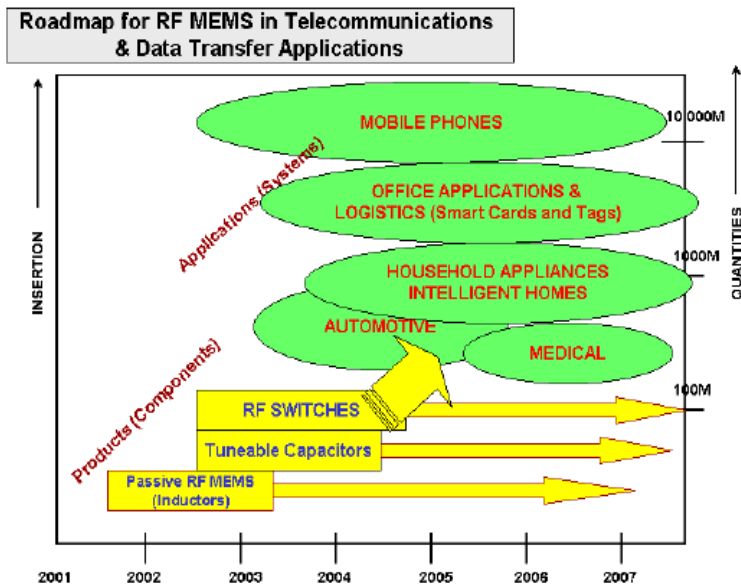


Fig 5 The RF-MEMS roadmap from the NEXUS Product-Technology Roadmap

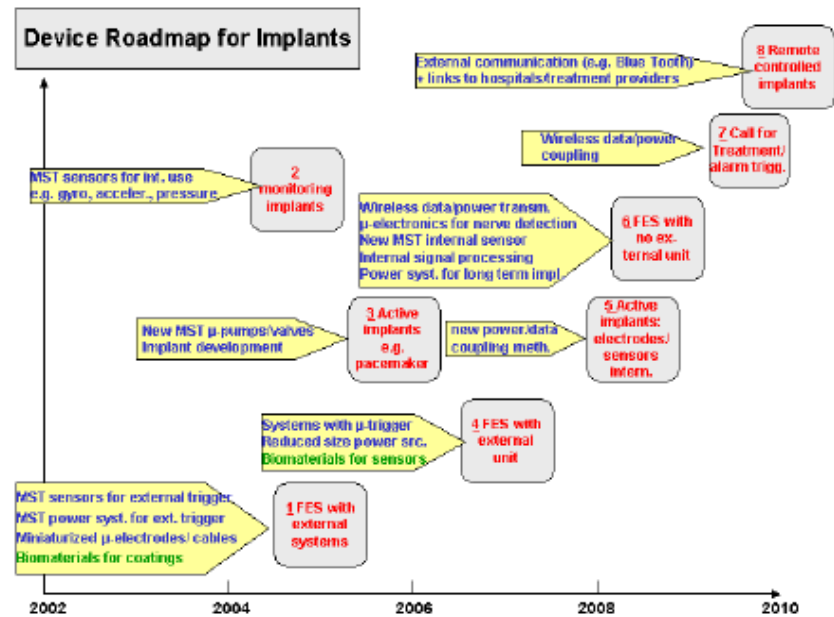


Fig 6 The device roadmap for medical implants from the NEXUS Product-Technology Roadmap

Source: NEXUS

Table 4: Packaging Challenges through 2007

Difficult Challenges (Through 2007)	Summary of Issues
Improved organic substrates	T _g (Glass Transition Temp.) compatible with lead-free solder processing
	Increased wireability at low cost, substrates are a barrier to flip chip adoption
	Improved impedance control and lower dielectric loss to support higher frequency applications
	Improved planarity and low warpage at higher process temperatures
	Low moisture absorption
Improved underfills for flip chip on organic substrates	Low-cost embedded passives
	Improve flow, fast dispense/cure, better interface adhesion, lower moisture absorption
	Higher operating range for automotive and Pb free soldering in liquid dispense underfills
Coordinated design tools & simulators to address chip, package, and substrate co-design	Improved adhesion, small filler size, and improved flow for mold based underfills
	Chip, package, and system level co-design tools
	Educational programs required to train engineers in co-design technologies
	Faster analysis tools for integrated thermal mechanical analysis
Impact of Cu/low κ (dielectric constant) on packaging	Higher accuracy, faster electrical simulation capability for high frequency design
	Direct wirebond and bump to Cu (Copper)
	Bump & underfill technology to assure low κ dielectric integrity
	Improved Mechanical strength of dielectrics
Pb (lead), Sb (antimony), and Halogen free packaging material	Interfacial adhesion
	Lower cost materials and processes to meet new requirements, including higher reflow temperatures.
Difficult Challenges (Beyond 2007)	
Package cost which may greatly exceed die cost	Reliability under thermal cycling (stress and moisture)
	Research investments required for packaging cost reduction are decreasing
Small, high pad count	Array I/O pitches below 80 microns
High Frequency die	Substrate wiring density to support >20 lines/mm
	Lower loss dielectrics
	Skin effect above 10Ghz

Table 93a Single-chip Packaging Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007
Technology Node	90nm				
DRAM % Pitch (nm)	100	90	80	70	65
Cost per Pin Minimum for Contract Assembly [1,2] (Cents/Pin)					
Low-cost, hand-held and memory	0.30-0.68	0.28-.58	.27-.50	.28-.48	.26-.45
Low-cost, hand-held and memory	--	0.30-53	.27-.50	.28-.48	.26-.45
Cost-performance	.75-1.30	.71-1.24	.87-1.17	.84-1.11	.81-1.05
Cost-performance	--	.71-1.24	.87-1.17	.84-1.11	.81-1.05
High-performance	1.88	1.88	1.78	1.89	1.81
Harsh	0.38-3.20	0.32-2.88	0.28-2.80	0.28-2.33	0.23-2.11
Harsh	--	0.32-2.88	0.28-2.80	0.28-2.33	0.25-2.11
Chip Size (mm ²) [3]					
Low-cost	100	100	100	100	100
Cost-performance	140	140	140	140	140
High-performance	310	310	310	310	310
Harsh	100	100	100	100	100
Maximum Power (Watts/mm ²) [4]					
Low-cost (Watts) [1]	2.5	2.7	2.8	3	3
Cost-performance	0.57	0.8	0.85	0.7	0.74
High-performance	0.48	0.61	0.64	0.58	0.61
Harsh	0.14	0.18	0.18	0.18	0.18
Core Voltage (Volts)					
Low-cost	1.2	1.2	1	0.9	0.9
Cost-performance	1.2	1.2	1	0.9	0.9
High-performance	1.2	1.2	1	0.9	0.9
Harsh	2.5	2.5	1.2	1.2	1.2
Package Pincount Maximum [5][6]					
Low-cost	112-408	122-500	134-550	144-800	180-880
Cost-performance	600-1462	500-1800	560-1780	560-1938	800-2140
High-performance	2400	3000	3400	3800	4000
Harsh	450	600	660	800	880
Minimum Overall Package Profile (mm)					
Low-cost	0.5	0.5	0.5	0.5	0.5
Low-cost	0.5	0.5	0.4	0.4	0.4
Cost-performance	1	0.8	0.8	0.8	0.8
High-performance	N/A	N/A	N/A	N/A	N/A
Harsh	1	0.8	0.8	0.8	0.8
Performance: On-Chip (MHz)[7]					
Low-cost	602/3184	562/3514	807/3886	888/4251	736/4878
Low-cost	602/3184	552/3200	807/3886	888/4251	736/4878
Cost-performance	3080	3880	6170	6830	8740
High-performance	3080	3880	6170	6830	8740
Harsh	72	80	88	88	108

†: Maximum power is average for die area

Manufacturable solutions exist, and are being optimized
 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known



Questionnaires + PATENT deliverables

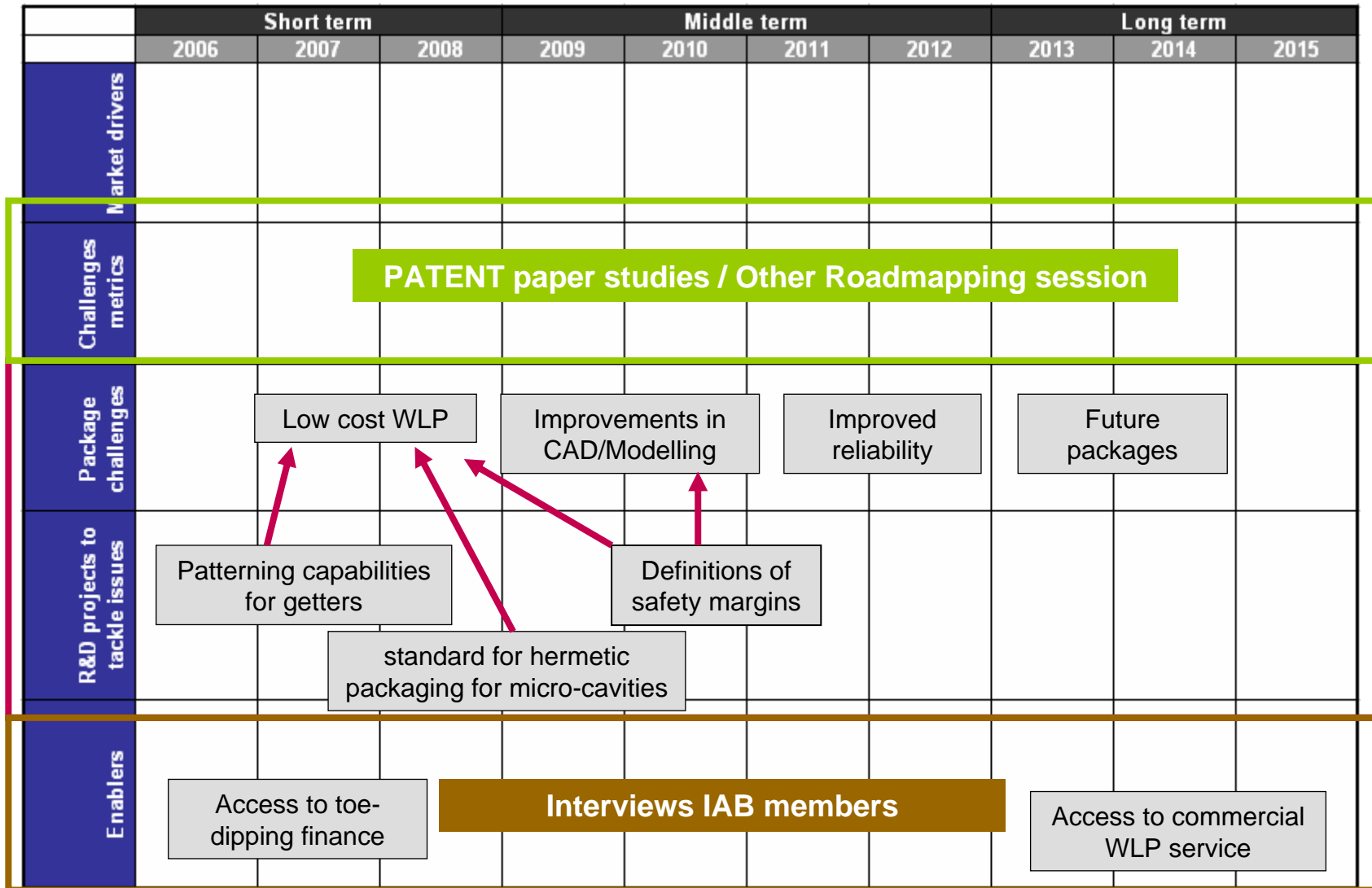


Summary of issues	(S)hort/(M)edium/(L)ong term	Priority (H / M / L)	RF / MOEMS / Both
Reducing costs of packaging	M/L	H	Both
Integrating active and passive components	M	H	Both
Development/integration of new materials for higher resonant frequencies	M	H	Both
Technologies that allow in-package tuning of RF devices	M	H	RF
Surface treatment of structures to prevent molecular absorption	S/M	H	RF



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- Today
 - Fill in the table

Summary of issues	(S)hort/(M)edium/(L)ong term	Priority (H / M / L)	RF / MOEMS / Both
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- After
 - Try and integrate metrics
 - Another event in Berlin (IZM)
 - Data checking by email
 - Final report

- Three "Thinking Sessions"
 1. Refine/expand list of difficult high-level challenges (11 for the moment)
 2. Each table allocated one challenge: What R&D projects could address these challenges?
 3. Each table allocated another challenge: What R&D projects could address these challenges?
- ... AND a live discussion

1- High-level challenges and summary of issues

~1 hour

List of High-Level Challenges and summary of issues



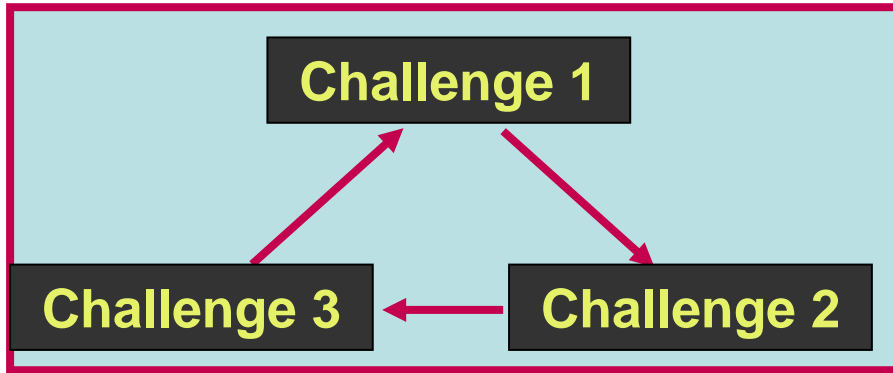
- Up to 15 minutes thinking
- 15 minutes group discussion
- 5x3mins reporting

FLIP CHART:

- Suggestions of different high-level challenges

COFFEE AND CHOOSE A TABLE

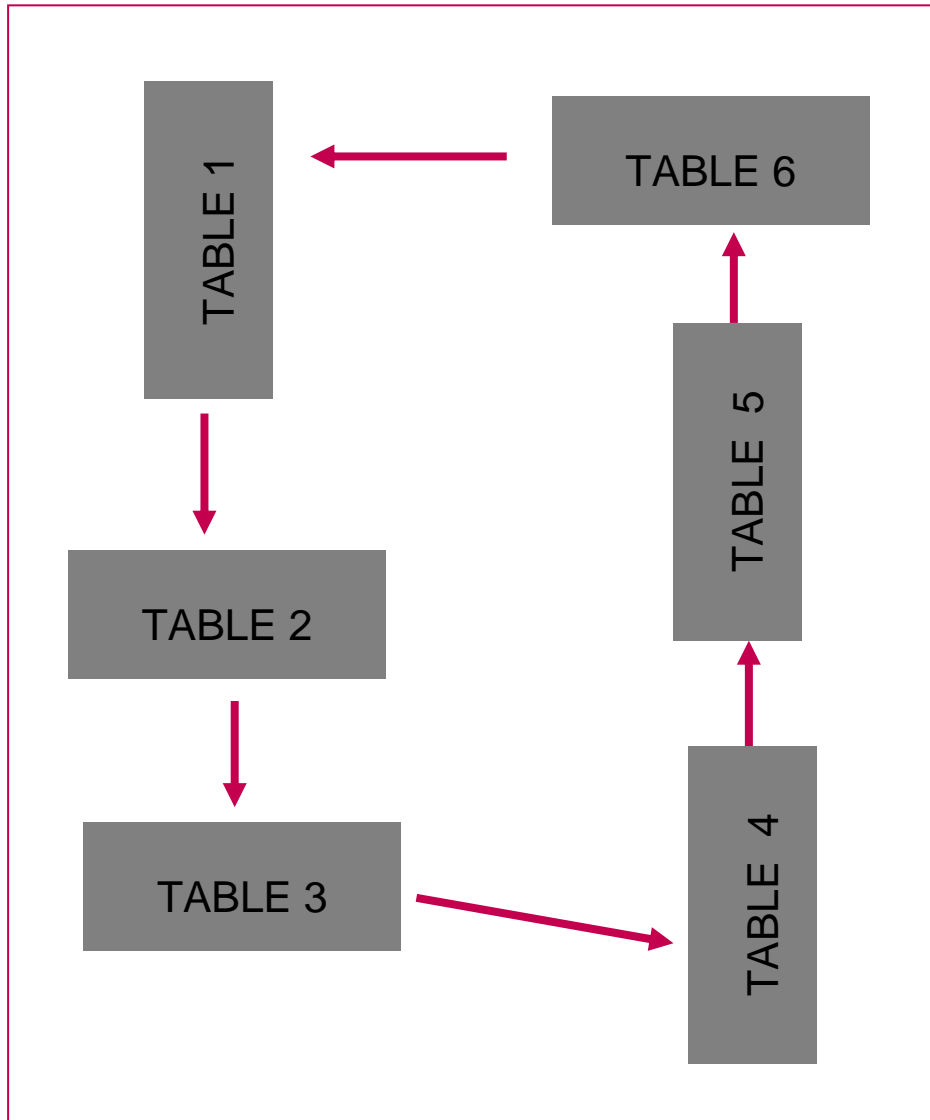
~1.5 hour



FLIP CHART:
 ~ 15 Major Issues to address
 (R&D projects, literature surveys...)

- Up to 15 minutes personal thinking: Major issues
- ↪ 15 mins: group discussion and Write up on Flip Chart
- 2 x 15 min rotation to other groups
- 25 minutes reporting

Summary of issues	(S)hort/(M)edium/(L)ong term	Priority (H / M / L)	RF / MOEMS / Both
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Development/integration of new materials for higher resonant frequencies	M	H	Both
Technologies that allow in-package tuning of RF devices	M	H	RF
Surface treatment of structures to prevent molecular absorption	S/M	H	RF



- **Leader stays at the table**
- **The rest of the group rotates**
- **15 minutes discussion around flip-chart**

Good luck!