To develop a methodology and initial tool-set for the assessment of the effect of packaging on the performance and reliability of MEMS devices

Cross work package activity
led from WP4

Jul-05

«Design for Micro & Nano Manufacture (NoE PATENT-DfMM)»
Network of Excellence funded by the European Commission (EC FP6 IST)

WP4 led, Cross WP research activity

- Packaging is often the least developed aspect of technology utilised to realise a system, often
  - resulting in a deleterious impact on the device performance and
  - giving rise to the main causes of long-term component failure
- These problems both slow the development of these devices, and their introduction into the market place.
- The PATENT-DfMM network provides an ideal view of the span of techniques available to assess the impact of packaging on MEMS components

Cross WP research activity

- Partners across all the four technical work packages will work together to develop techniques to assess the impact of packaging on both the performance and reliability of MEMS devices
- The ultimate aim of the activity is to incorporate these assessment techniques into a methodology for the realisation of reliable packaged microsystem devices
  - Funding routes for the demonstration of such a methodology will be investigated in a separate linked programme funded by WP7
- The availability of such a methodology will put the European Community in a strong position with respect to the commercialisation of MEMS components

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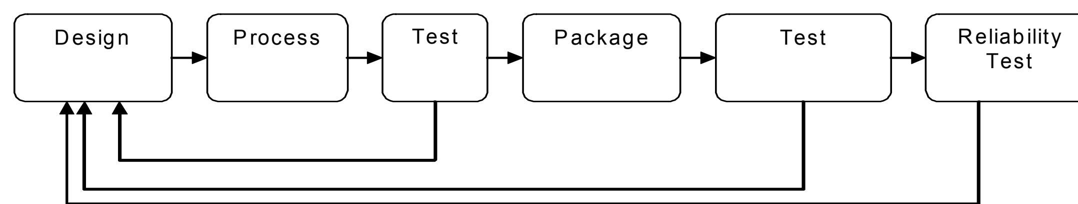
Cross WP research activity

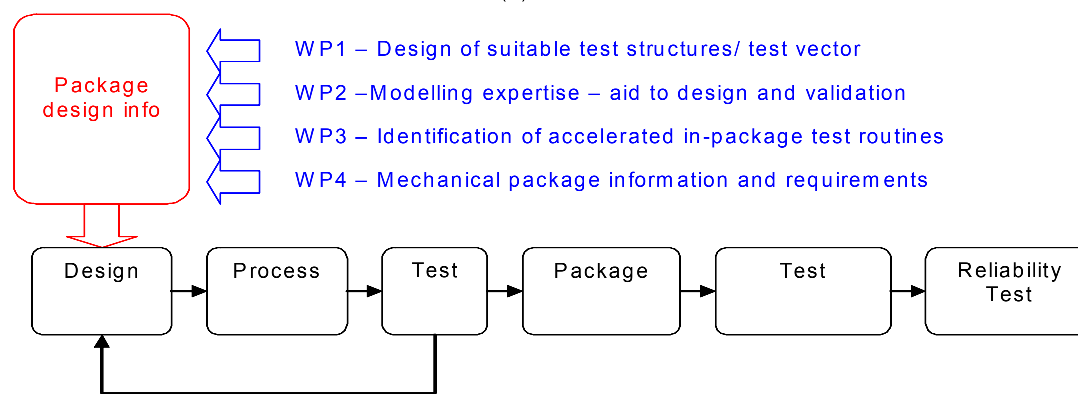
- This will be achieved through a combination of
  - improved modelling and simulation of the device package interaction, and
  - the use of specifically designed test structures allowing the measurement of key parameters relating to the package environment, such as stress and pressure.
- As most component packages will be opaque proposed to concentrate on electrical techniques
- The use of such test structures will enable rapid assessment of the impact of any given packaging technology on a MEMS components performance and reliability both
  - during the design phase, and
  - during its operational lifetime

Overall Aim

- The aim of the overall activity is to incorporate these assessment techniques into a methodology for the realisation of reliable, packaged mircosystem devices.
- Initially arrays of test structures will be used to fully understand and quantify the effect of different packaging on the MEMS components.
  - Use arrays of test structures rather than real devices (ideally same die size and technology as device to be packaged, but not necessarily)
    - yield quantitative data on the environment within the package
    - rather than trying to interpret the effect of the packaging from the observed effect on the device
  - Test structure arrays could be used to assess/ screen different packaging
- The effect of the packaging on the test structures will also be modelled. The quantitative data from the measurements will be feed back, to improve the modelling and simulation.
- Ultimately once the process is complete the process can be done entirely within the modelling and simulation environment.



(a)



(b)

Process flow for a) traditional and b) improved methodology for design of microsystems showing cross WP inputs.

Partners

- **QinetiQ,**
- **University of Lancaster (ULAN)**
- **NMRC**
- **Fraunhofer IZM, Berlin**
- **Fraunhofer IZM, Munich**
- **IMEC**
- **Heriot Watt University**
- **Politecnico Di Milano (POLIMI)**

Deliverables

- A proposed "first draft" best practice methodology for assessing the effect of packaging on the performance and reliability of MEMS components. This will be based on
  - a review of the current state-of-the-art undertaken by participating partners and
  - some simple first order experiments on to validate work being undertaken within WP2 on improved modelling and simulation of the device package interaction
- Identification of gaps in expertise/ areas where significant technical progress can be made within the group.
  - These may be improved modelling techniques, measurements techniques and test structures and/ or access to suitable materials data.
- It is anticipated that this will lead to a number of spin-out/ follow up projects resulting from the activity. Some to be funded externally to PATENT, bringing additional resources into the PATENT consortium.

Modelling and simulation activities

- Review of state-of-the art modelling of the device package interaction
- Improved modelling and simulation of the device package interaction by
  - combining the expertise at the various partner sites
  - to develop and demonstrate efficient simulation methodologies for modelling of MEMS devices,
    - including faults, under packaged conditions
- Testing of concepts where feasible
  - Modelling
  - Physical testing
    - Expertise on and access to test capabilities for package testing – IMEC, IZM
- Review of commercially available solid models for packages
  - assessment of Coventor/ Kyocera package library

Demonstrator devices for modelling and physical verification

- RF switch test structure array to assess the effect of packaging on pull-in voltage
  - Simulation of packaged components including realistic models for attach layers
- Non-linear shuttle resonator
    - Spring stiffness increases with deflection
- Electronic readout version of standard bent-beam strain sensor

  - **Design and measured data exchanged to allow comparison different modelling techniques/ methods**
  - **Modelled results compared to physical measurements**
  - **Establish/ identify best practice**
- Packaging activities encouraged to use packages from the Coventor/ Kyocera package library
  - Specific evaluation of package library using QinetiQ RF switch

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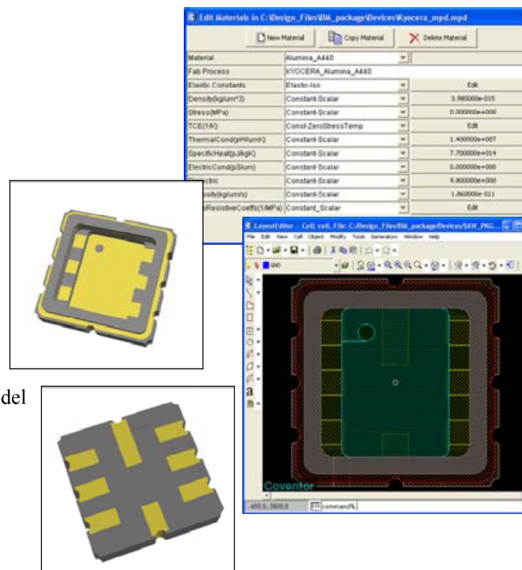
Review of commercially available solid models for packages

KYOCERA Package Library for CoventorWare

- Deliverables:
- Package Models
  - SMD (Surface Mount Device)
  - S/B (Side Braze)
  - PGA (Pin Grid Array)
  - C-DIP (Cerdip)
  - LCC (Leadless Chip Carrier)
  - F/P (Flat Pack)
  - CSP (Chip Scale Package)
    - Layout files (.cat, .dxf)
    - Process emulation files for 3D model generation
    - 3D SAT
- Package library user interface
- Material Property database
- Supplemental documentation



Slide courtesy of Coventor

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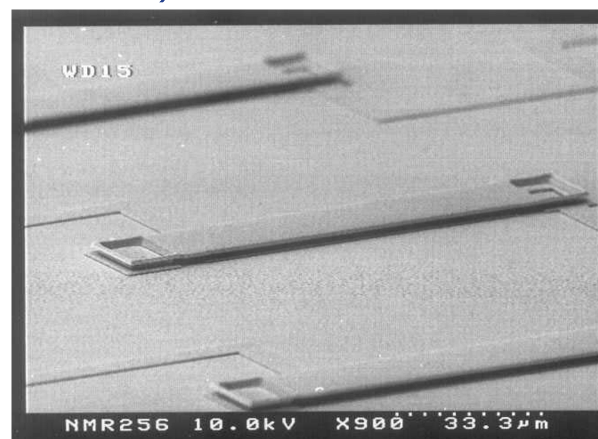
Device 1

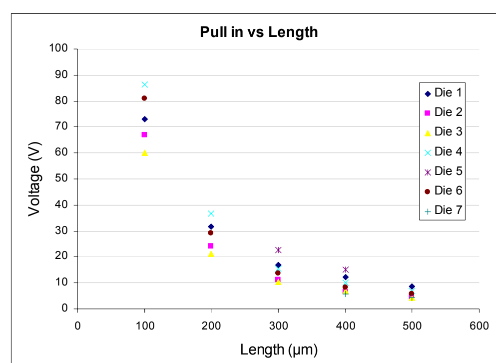
- RF switch test structure array to assess the effect of packaging on pull-in voltage
- The samples consist of fixed-fixed beams,
  - ranging from 100 to 500um in length.
  - three different anchor variations and
  - three different widths (10-20-50um).
- Initial pull-in voltages
  - Range from 4-100V
- Key Issue
  - Adhesive die attach
    - Accurate data
    - Accurate modeling

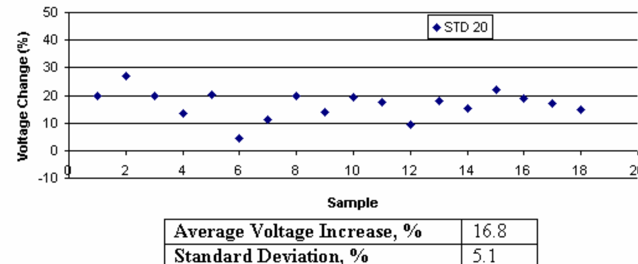


Device 1

- Characterisation of adhesive die attach using test sample to input to modelling
  - Test structure created for adhesive die attach characterisation
  - Initial adhesive characterised
  - Additional adhesives to be characterised
- Measurements pre-and post- packaging to compare to / verify modelling
  - Electrical – pull in voltage
  - Out of plane deformation measurements
  - RAMAN (surface and cross sectional) and curvature measurements on correct size, but thinned plain silicon die (to maximise effect)
- To use Kyocera PGA packages from the Kyocera package library in Coventorware
  - Modelling of device package interaction in Coventorware using appropriate package model

Device 1 - Pre and post packaging pull in measurements





Average Voltage Increase, %	16.8
Standard Deviation, %	5.1

- Measurements carried out before die attach

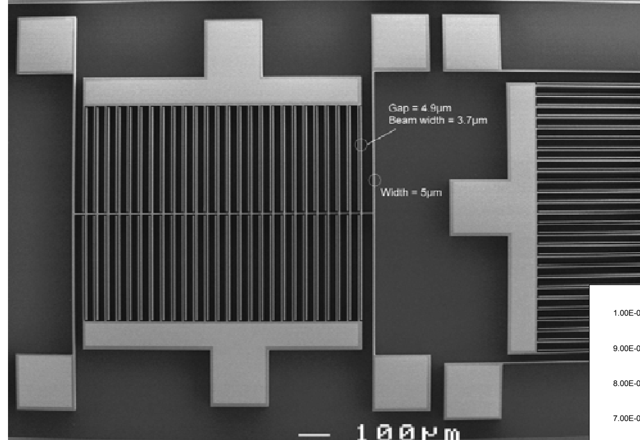
- Measurements carried out after die attach
- Threshold voltage increased
- Increase in structural stress of ~10MPa

Modelled using Ansys, Coventor, Intellisuite

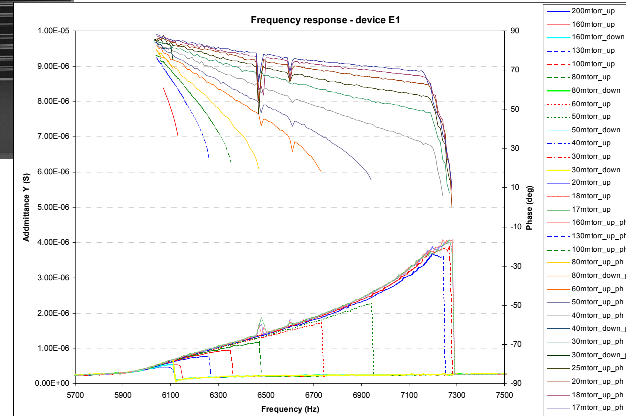
Device 2

Measurements carried out on packaged, non-linear shuttle resonator

- Resonant Magnetometer



Packaged Non-Linear Shuttle Resonator, measured at QinetiQ



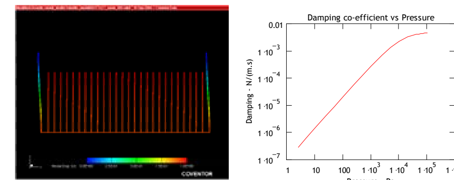
Device 2

Modelled using

- Ansys,
- Coventor,
- Cosserat Theory (ULANC),
- BEM (POLIMI)

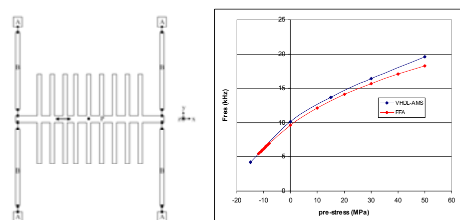
Demonstrator 2

- Coventorware modelling carried out
  - Modal and damping



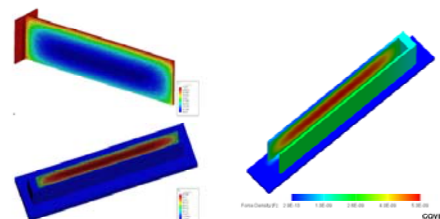
Demonstrator 2

- Reduced order model implemented using Cosserat theory
- Packaging stress approx. -10MPa



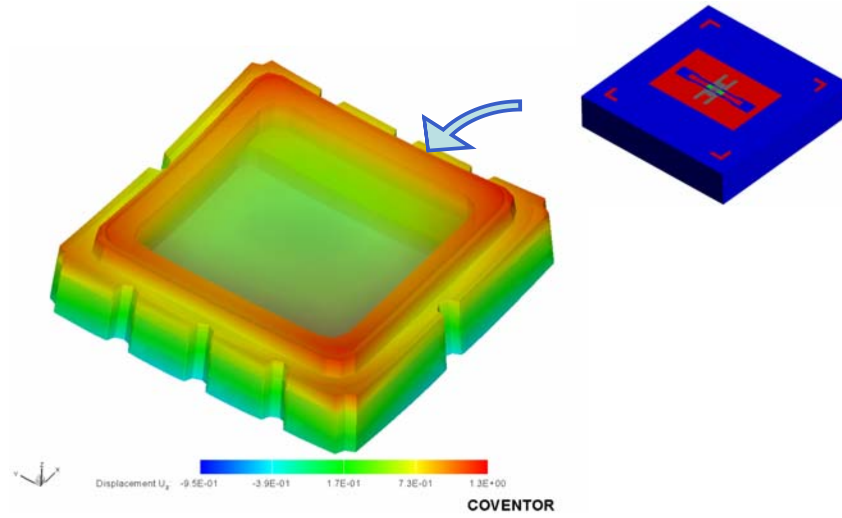
Demonstrator 2

- BEM damping simulations using POLIMI models and Coventorware simulations

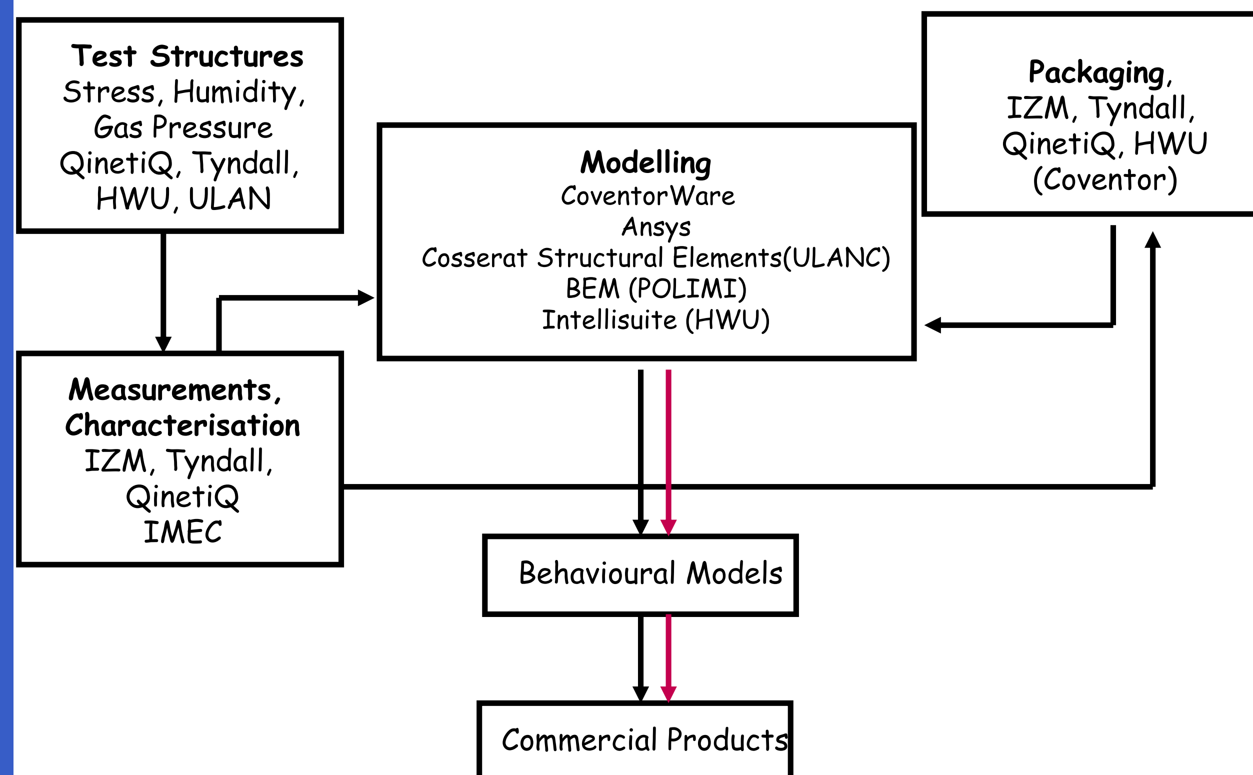


Package library

- Evaluation of Coventorware package library underway with support from WP4
  - To use Kyocera SMD 99902-A
- Application – QinetiQ RF switch



Demonstrator device activities



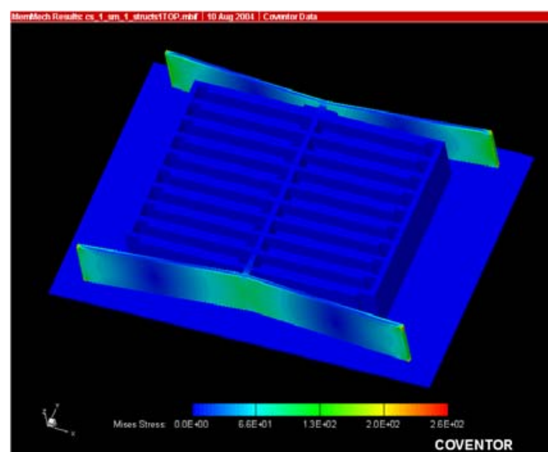
Test structure arrays for quantitative physical measurement

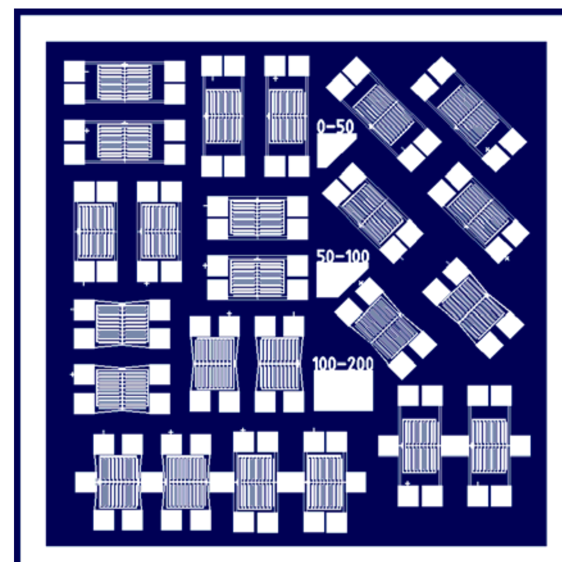
- Review of key packaging related parameters affecting performance and reliability of MEMS devices
- Review of package related failure modes
- Review of devices for in package monitoring, including
  - Package stress monitoring
  - Pressure monitoring
  - Humidity monitoring

  To include any commercially available devices for in-package monitoring.
- Review of accelerated life test techniques for package related failure modes

In-package stress test device

- Capacitive readout strain sensor designed, modelled and fabricated - awaiting package & test





Future & Linked Activities

- Spin-out/ follow up projects
  - Following identification of gaps in expertise/ areas where significant technical progress can be made within the group
    - Broader application range & additional test structures
    - More on Die attach/ Adhesives
    - In-package humidity sensors
  - Possible activity to demonstrate the methodology
    - Funding required beyond that available from PATENT-DfMM
    - Need to seek significant funding from some other funding source
- Training course development
  - MEMS Packaging, Modelling and Test,
    - Fraunhofer IZM Berlin (lead), IEF, Heriot Watt, Lancaster University, IMEC

Future demonstrator activity

- Plan to exploit 1st phase of the cross work package activity
  - on assessment of stress, pressure, humidity
- Demonstrate methodology for packaging of accelerometers and gyroscopes
  - specifically designed test structures allowing the measurement stress, pressure and humidity
  - Improved modelling and simulation
    - Extra work on modelling of leak rate/ moisture ingress
- Looking at variety of packaging types
  - TO Cans, Ceramic LCC, bare die in plastic, wafer level packaging, packaging of thinned devices (Tyndall)