



WP1: Design for Testability of Micro- and Nano- Systems

Latest Advances in MEMS Testing

May, 30th, 2005 – Montreux

Moderator: Andrew Richardson, University of Lancaster



LANCASTER
UNIVERSITY

MESA+



Institute for
System Level
Integration
THE ALBA CAMPUS

QinetiQ

«Design for Micro & Nano Manufacture (NoE PATENT-DfMM)»

Network of Excellence funded by the European Commission (EC FP6: IST, Unit C2, Contract 507255)



Workshop schedule

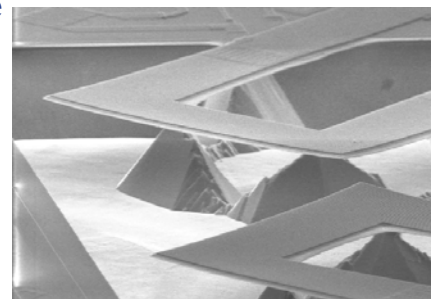
Network of Excellence «Design for Micro & Nano Manufacture (NoE PATENT-DfMM)»
Workshop on "Latest Advances in MEMS Testing"

www.patent-dfmm.org
Jun-05 Slide 2

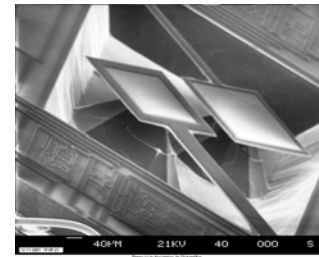
- 14h00
Welcome address and WP1 activity overview
Pascal Nouet, WP1 leader
- 14h15
DfT for Biosensors
Hongyuan Liu, University of Lancaster
- 14h35
Bias superposition for MEMS Testing
Frederick Maily, LIRMM, Univ. of Montpellier II
- 14h55
On-chip testing for mechanical characterization of thin polysilicon films
Alberto Corigliano, Politecnico di Milano
- 15h15
Mini-panel
all presenters

- Design for testability of MNS
 - Everything that may improve testability of a MNS by an action during the design phase
 - Reduction of Go/noGo test costs – Self-test
 - Fault tolerance – Self-repair
 - Reduce requirements for functional testing – Self-calibration
- To build a virtual laboratory (20 researchers)
 - Integration of research – joint research
 - contribution to training and dissemination

- **Cost of external test stimuli:** Acceleration, temperature, magnetic field or any other physical magnitude are expensive stimuli to generate. Alternative methods to stimulate MNS inputs using electrical signals will be considered.
- **Cost of specification-based tests:** for complex systems, it has been demonstrated that it is generally cheaper to verify the physical integrity of the device rather than its functional behavior (→ Structural Testing).
- **Impact of packaging on test costs:** it is generally necessary to test packaged devices and numerous bad devices are then packaged to be rejected after.
- **Nanosystem specificities:** emerging technologies are generally exhibiting low yield. It is then mandatory to develop fault tolerance scheme to make a system working with faults (use of spare cells).
- **Low-cost test methodologies:** by reducing the demands on ATE, BIST will strongly reduce test costs. On-line testing, self-calibration, self-repair, ...



- 3 research projects
 - ▶ ■ Q-factor monitoring
 - ▶ ■ Bias superposition
 - ▶ ■ DfT for Biosensors
- 1 preliminary study (MEMS Benchmarking)
- ▶ Literature database
- ▶ Other 2004 achievements
 - Integration of research
 - Performance indicators
 - Conceptual Product Portfolio



- Measure / Characterize Q values
- Numerous potential applications for generic methods
 - PCM: QFM to get precise information on eventual defects during fabrication stages, vacuum package hermiticity
 - End of line testing: low-cost detection of out of range values
 - On-line: failure detection, fatigue, drift compensation, self-calibration



- Bias Superposition
 - Altering the bias of a sensor to extract the measurement data **and** an indication of the sensor's health
 - Uses out-of-bandwidth signals to enable filtering of signal
 - Complex biasing schemes can be multi-physical
 - Electric, Thermal, Magnetic
- Theoretical studies
 - Potential application to wheatstone bridges
 - State of the art in self-test of capacitive sensors
- Test Cases: application to two sensors



- Motivations
 - DNA sensors are a large potential market
 - Array-based sensors require fault-tolerant schemes / management of spare cells
 - DfT solutions are few only and must be adapted from specific works on μ Fluidics
 - WP must develop some skills in this field
- Project objectives
 - Define a test case and potential DfT solutions
 - Explore potential partnerships



- Integration of research
 - Virtual lab: partners must share background knowledge
 - Review paper ; common tutorial on state of the art ; common material for academic courses
- Expertise demonstration
- As a service to industry
 - Free access to registered users in an early phase
 - Restricted access to « customers » in the self-sustainable phase

- 2004 Achievements
 - Collection of about 100 papers
 - Paper reviewing and indexing
 - On-line database (WP1 only)
- 2005 objectives
 - Database available to public next summer (inc. search engine)
 - Advice request available end of 2005 (question to a WP1 expert)
 - 20-30 new papers
 - 1-2 white/review papers

- Some of the task force members collaborate in projects funded by other WP but closely linked with WP1:
 - **Fault Modelling** and System Simulation of Flow-FETs (WP2)
Participants: **MESA**, CCLRC & IMT.
 - **MEMS Testing** by Electro-Thermal Excitation (WP7)
Participants: **LIRMM**, BUTE, TIMA and MICRED
 - Methodology for reliable, packaged of Micro and Nanosystems
Participants: **QinetiQ**, **University of Lancaster**, IMEC, NMRC, HWU, Fraunhofer IZM and Politecnico di Milano
- Dissemination / training
 - Half day tutorial at the 2004 summer school
 - Embedded tutorial at ETS 2005
 - Publications in main 2005 conferences (DTIP, ETS, VTS, IMSTW...).



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