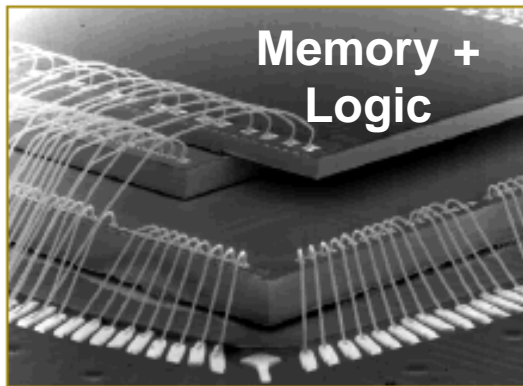


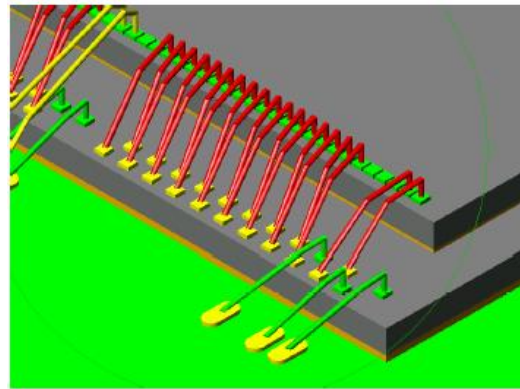
Modelling Methodologies for Reliability and Prognostics of SiP Structures - Current Capabilities and Future Challenges.

Chris Bailey, Stoyan Stoyanov

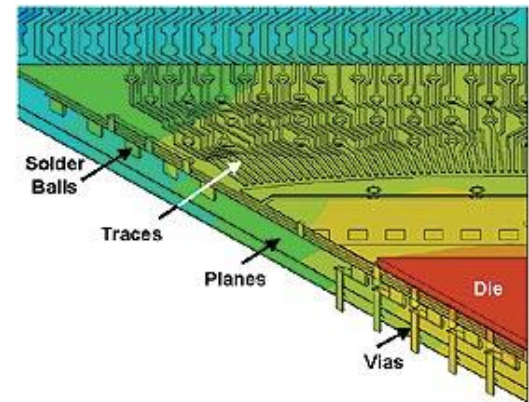
****University of Greenwich, London, UK***



Real World



Physical Layout



Simulation/Analysis

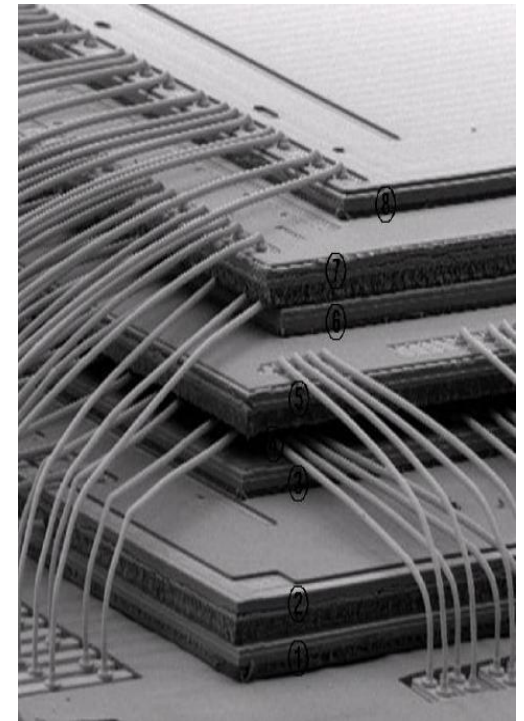
Acknowledgements

- Number of projects supported by UK Government and Industry in Collaboration with:



Content

- **What is System in Package (SiP)**
- SiP Design Challenges
- Modelling Technologies to support DfX
- Examples
 - Design for Reliability
 - Design for Manufacture
- Modelling tools for Prognostics
- Future Challenges
- Conclusions



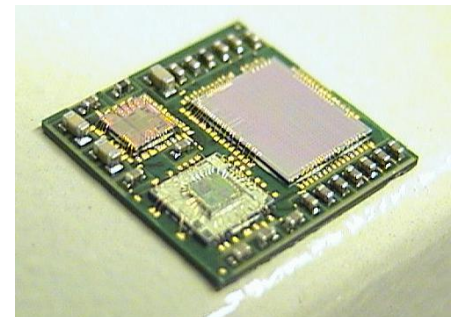
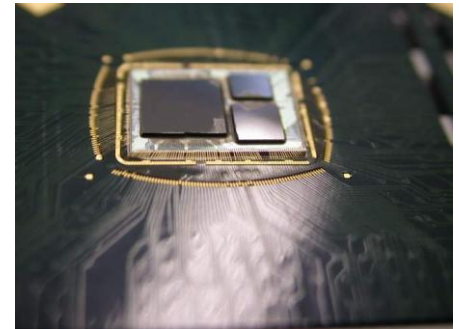
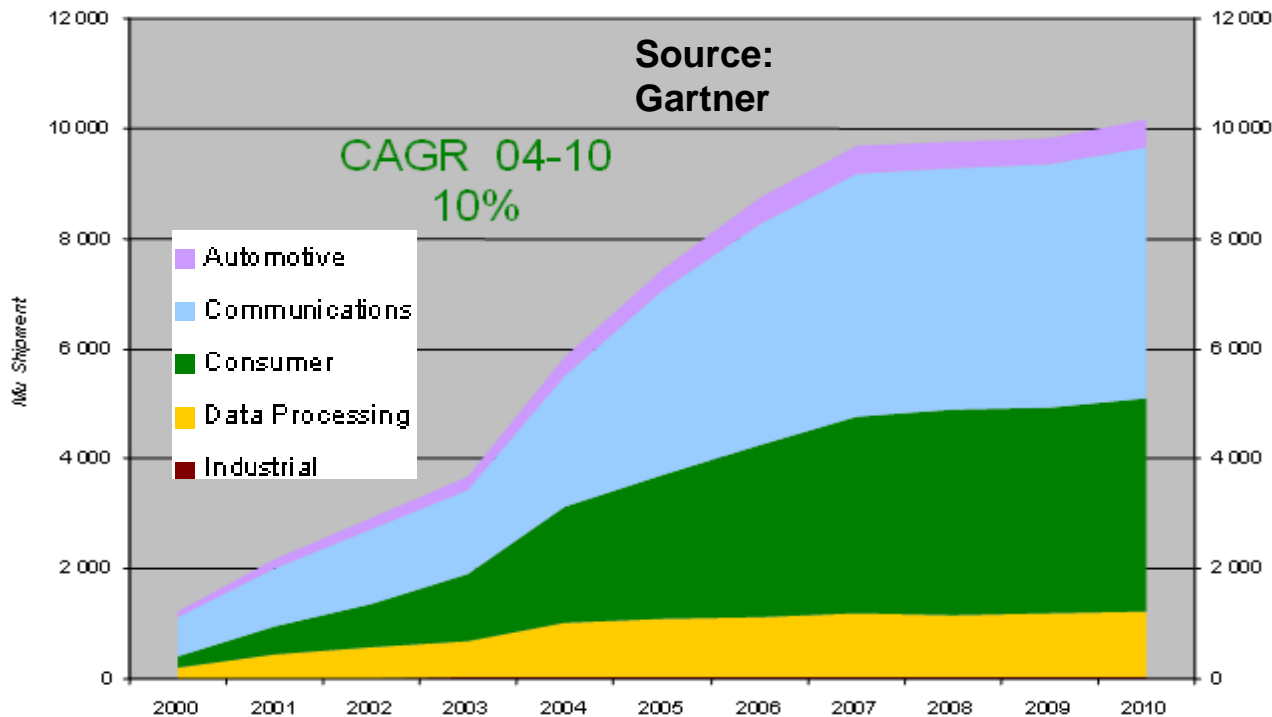
What is SiP



- ITRS

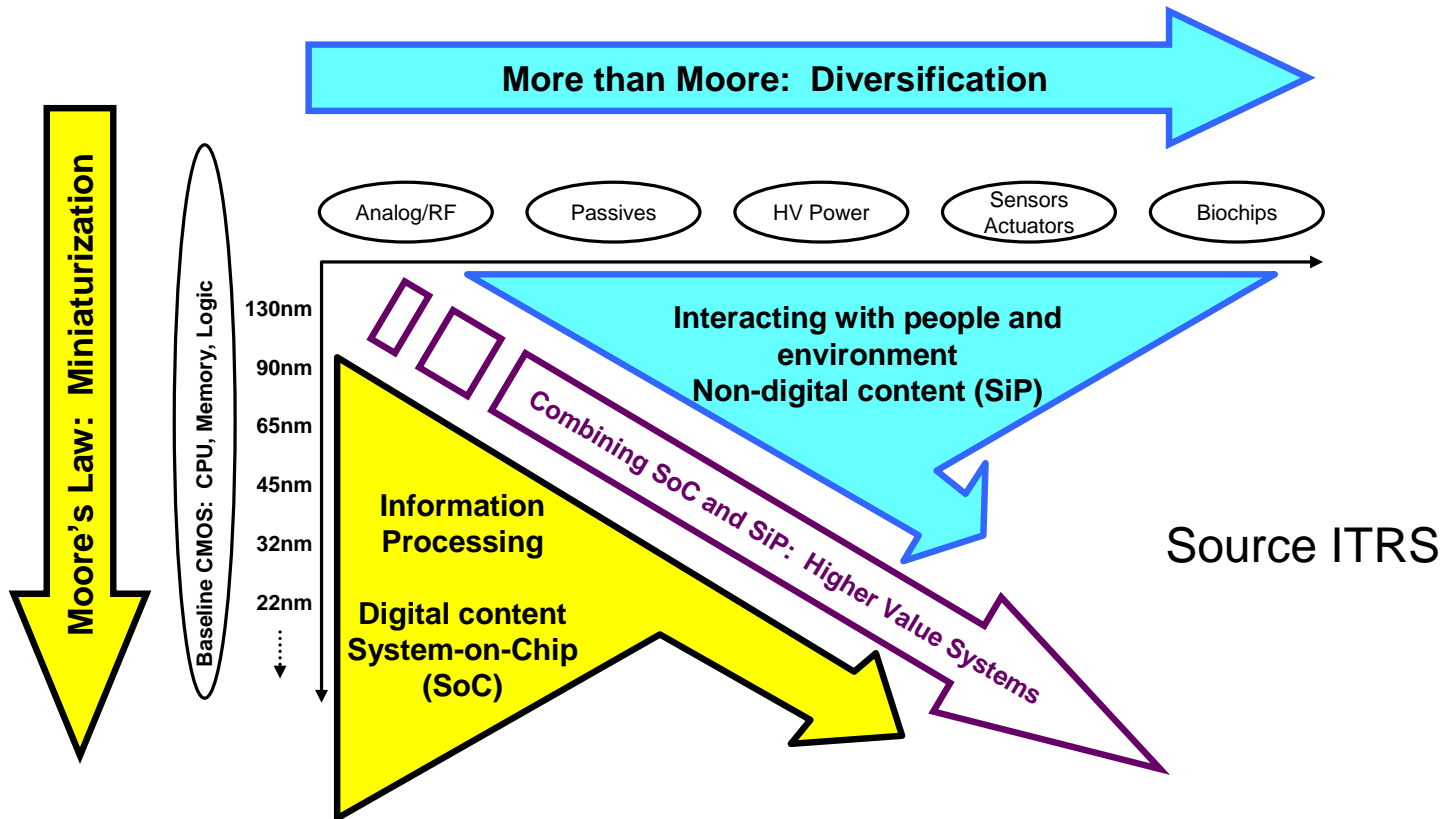
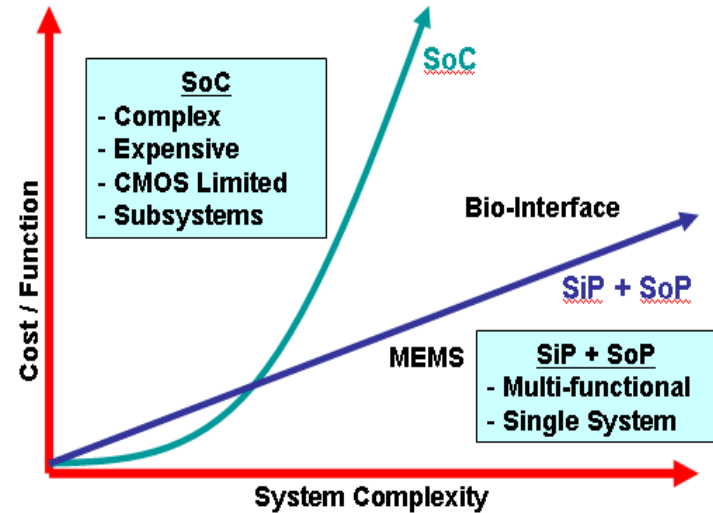
– “Any combination of semiconductors plus optionally other components such as passives, MEMS, and optical components assembled into a single package”

SiP Market Projection



Why SiP

- Size & Complexity Reduction
- Reduced Design Effort Cost
- Lower System Costs
-



Packaging Types - SiP






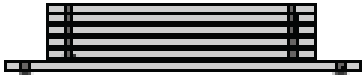
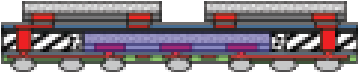
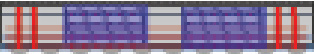

Horizontal Placement		 Wire Bonding Type		 Flip Chip Type			
Stacked Structure	Interposer Type	 Wire Bonding Type		 Wire Bonding + Flip Chip Type		 Flip Chip Type	
	Interposer-less Type	 Terminal Through Via Type					
Embedded Structure		 Chip(WLP) Embedded + Chip on Surface Type			 3D Chip Embedded Type		
		 WLP Embedded + Chip on Surface Type					

Figure AP15

Categories of SiP

Source ITRS

Through Silicon Via

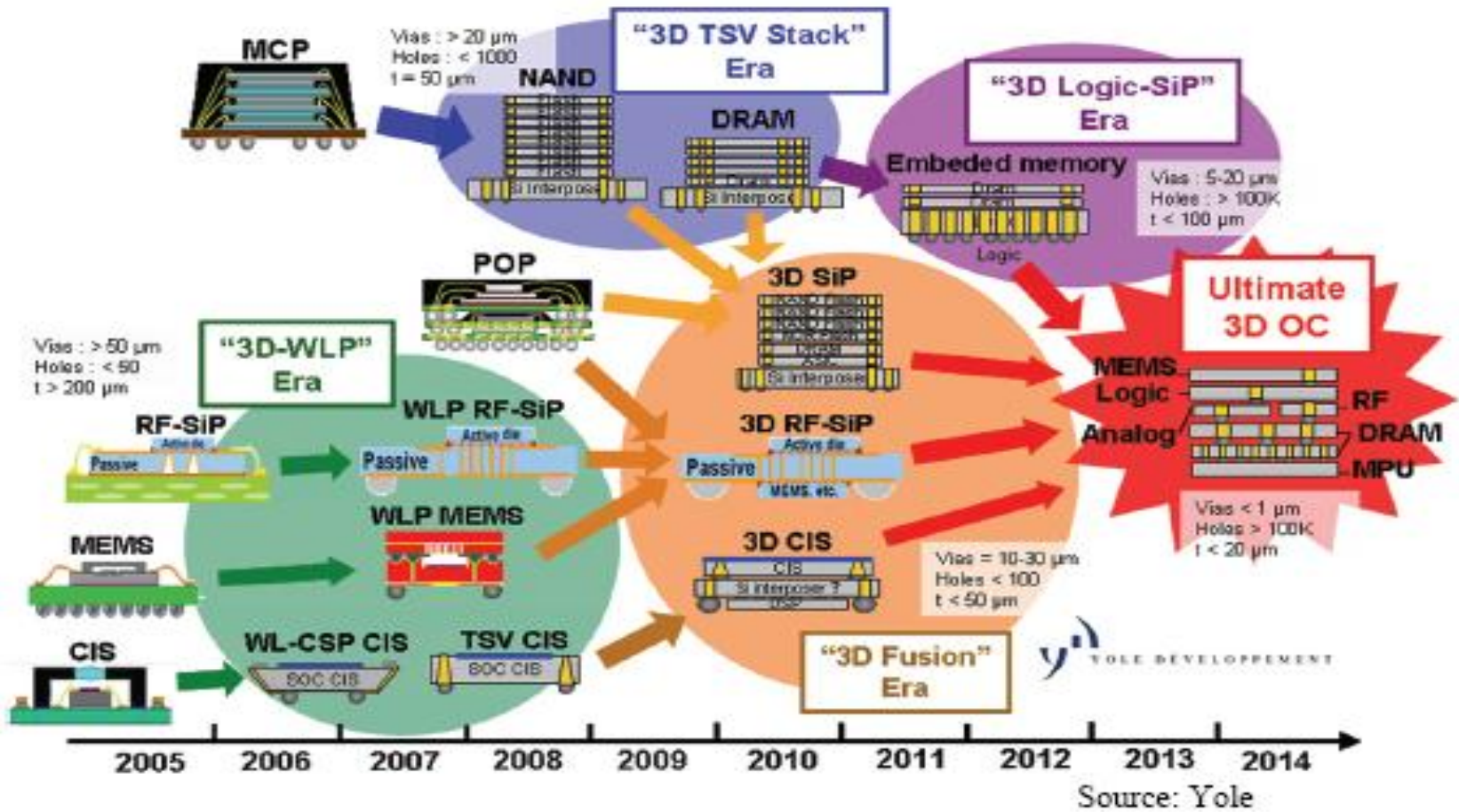
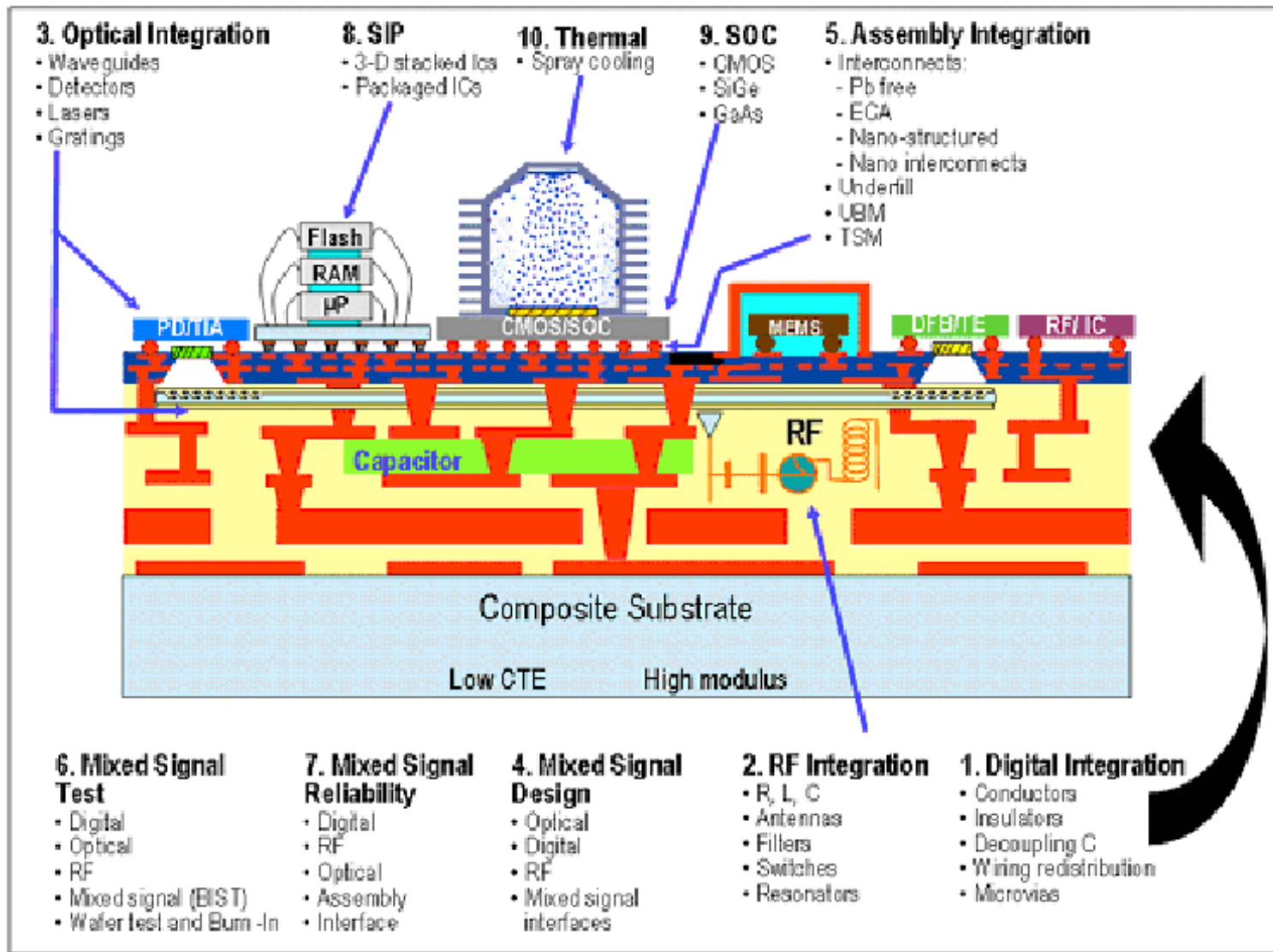


Figure AP12

Roadmap for 3D Integration using TSV

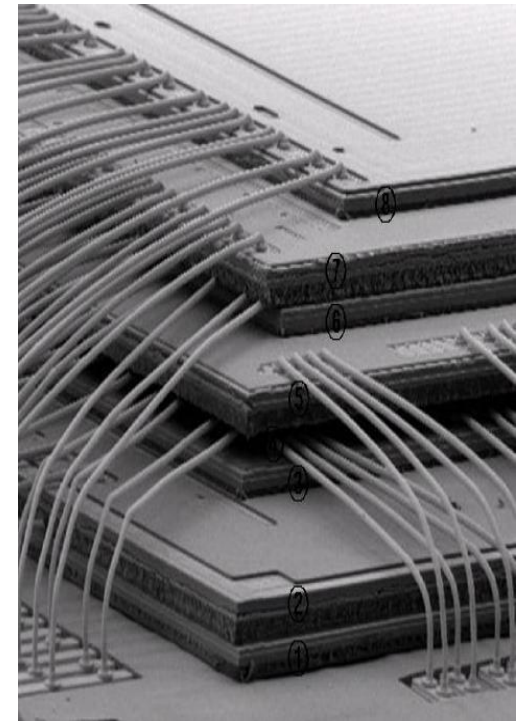
SoP Vision of the Future



Source: Professor Rao Tummala, Georgia Institute of Technology-Packaging Research Center.

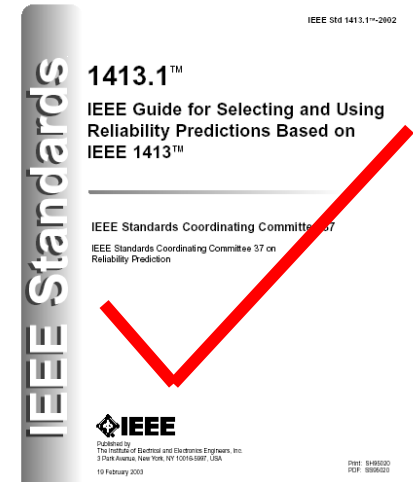
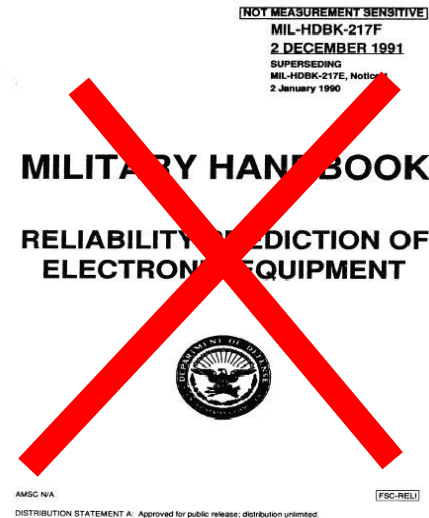
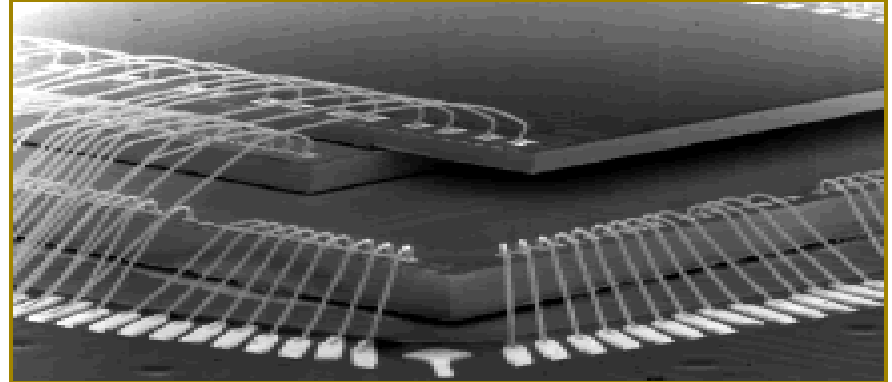
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- What is System in Package (SiP)
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- Examples
 - Design for Reliability
 - Design for Manufacture
- Modelling tools for Prognostics
- Future Challenges
- Conclusions



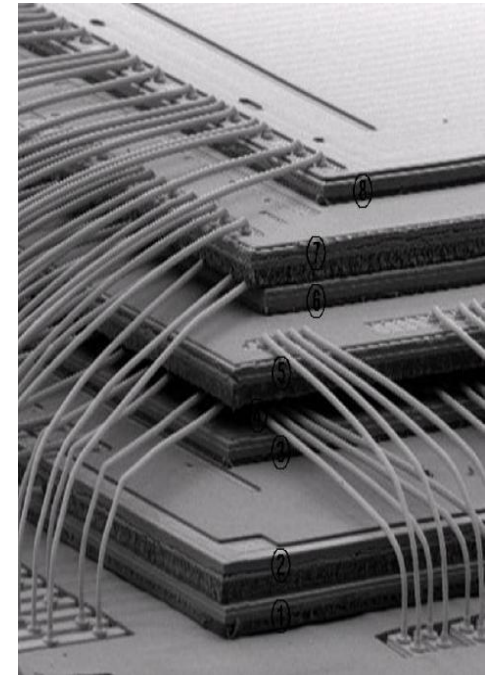
Challenges - SiP

- Physical Design
 - 3D Rule Checks
- Electrical
 - Complex routing
 - HD Boards: Crosstalk, Coupling....
- Thermal
 - Multiple heat sources
 - Lots of interfaces
- Reliability
 - New failure Modes
 - New Materials
 - Acceleration Factors



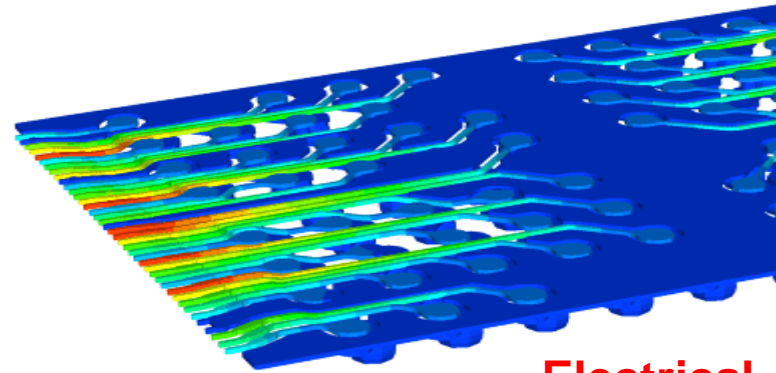
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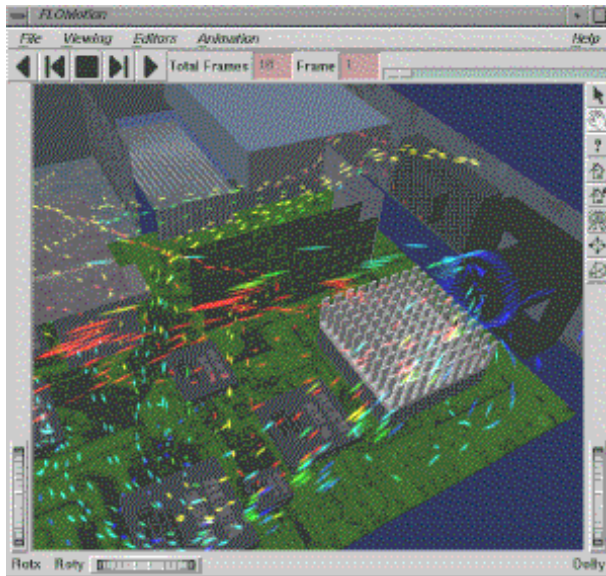


Modelling Tools – High Fidelity

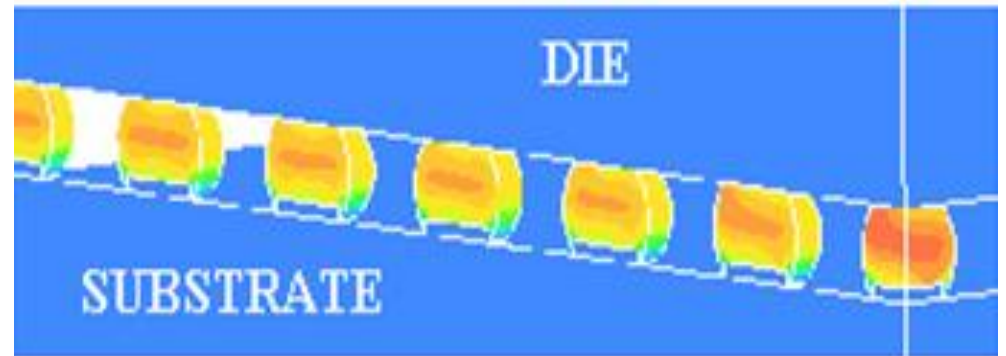
- High Fidelity Tools (FEA, CFD, etc)
 - Electrical, Thermal
 - Mechanical



Electrical



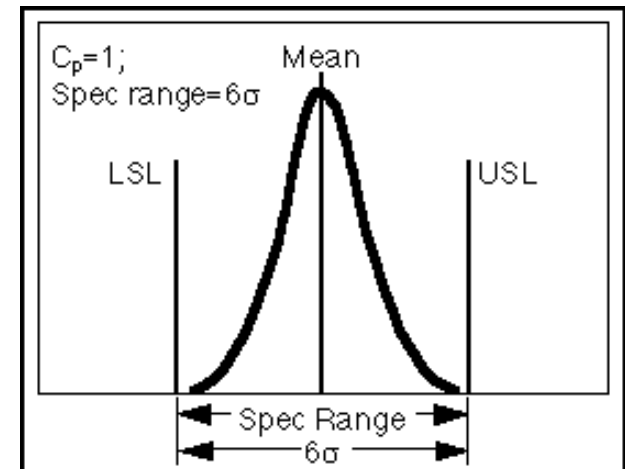
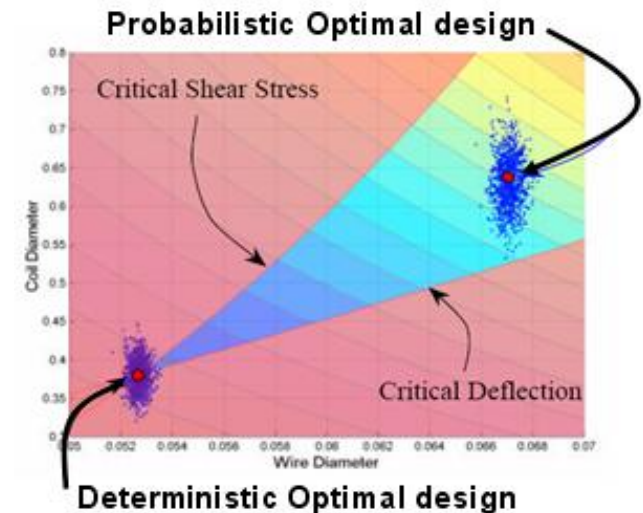
Thermal



Mechanical

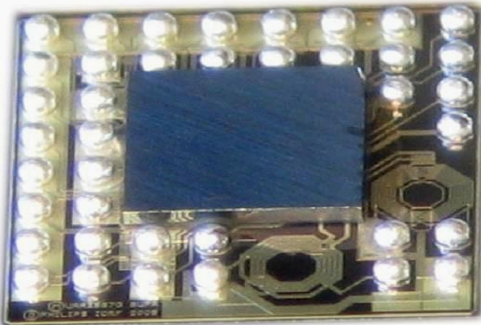
Modelling Tools – Optimisation and Reduced Order

- Optimisation
 - Design of Experiments
 - Sensitivity Analysis
- Reduced Order Modelling
 - Compact Models; Krylov Subspaces, Cosserat Theory, Response Surfaces
 - Fast Analysis
- Uncertainty and Risk Analysis
 - Monte Carlo, First and Second Order Moment Methods



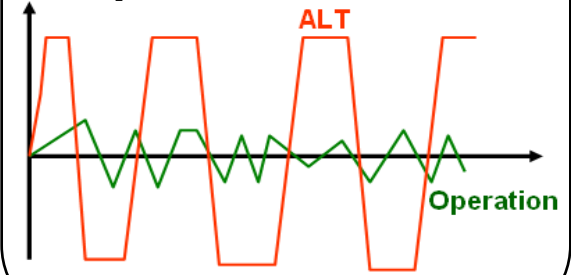
Physics-of-Failure Reliability

Hardware Configuration



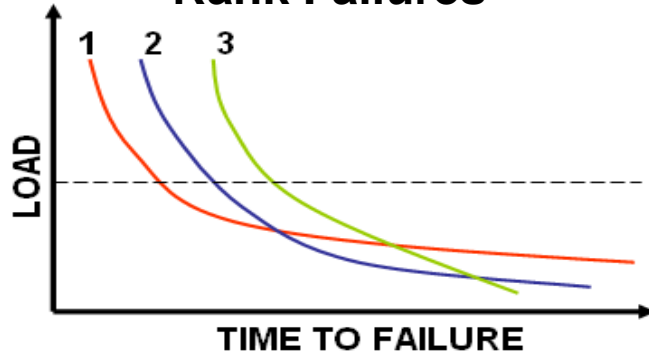
Stress Analysis

Accelerated Test Loads
Operational Loads

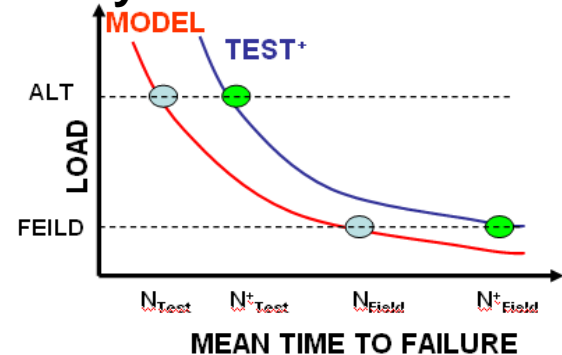


Apply Damage
(PoF) Model

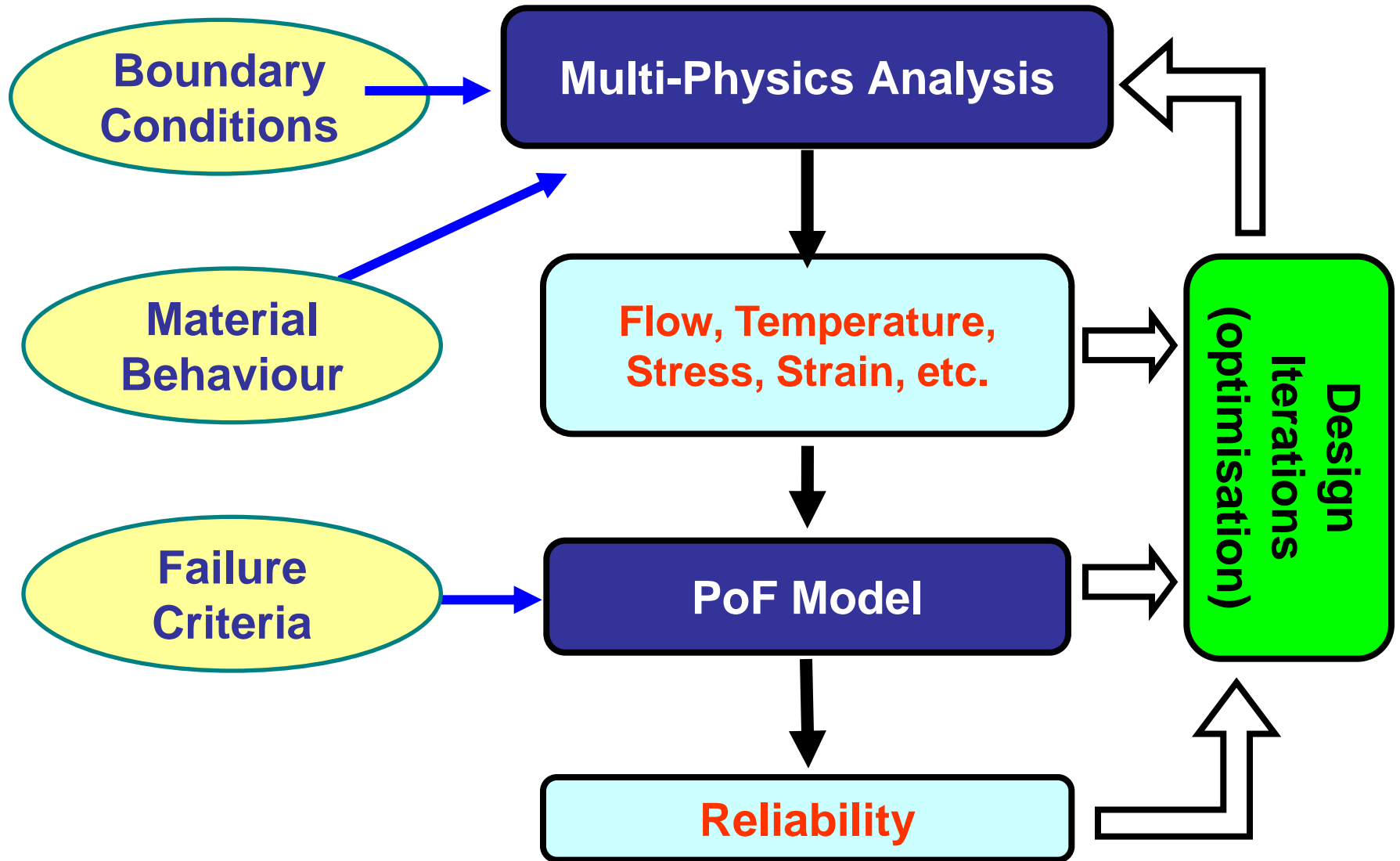
Rank Failures



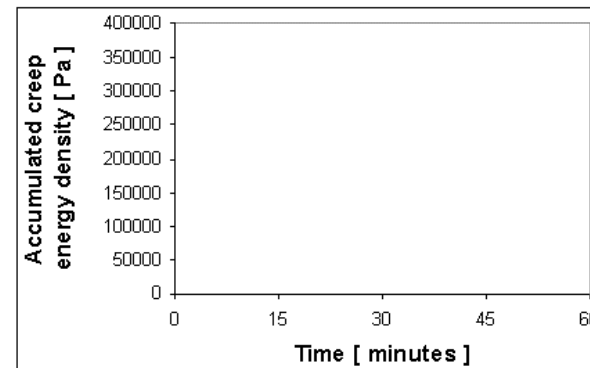
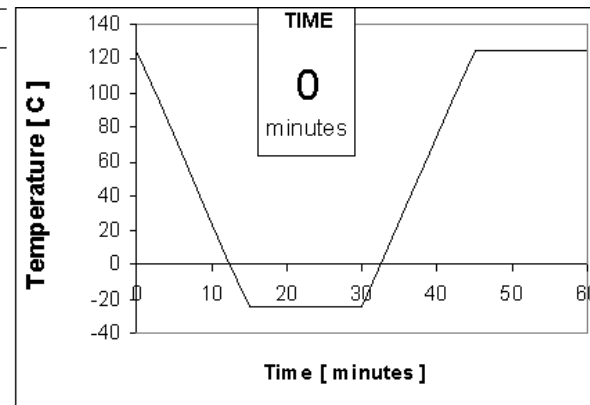
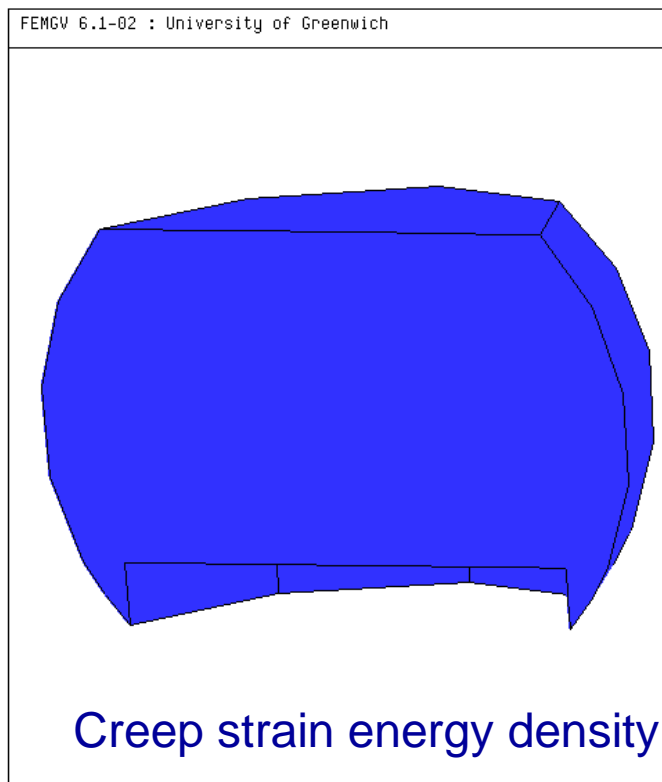
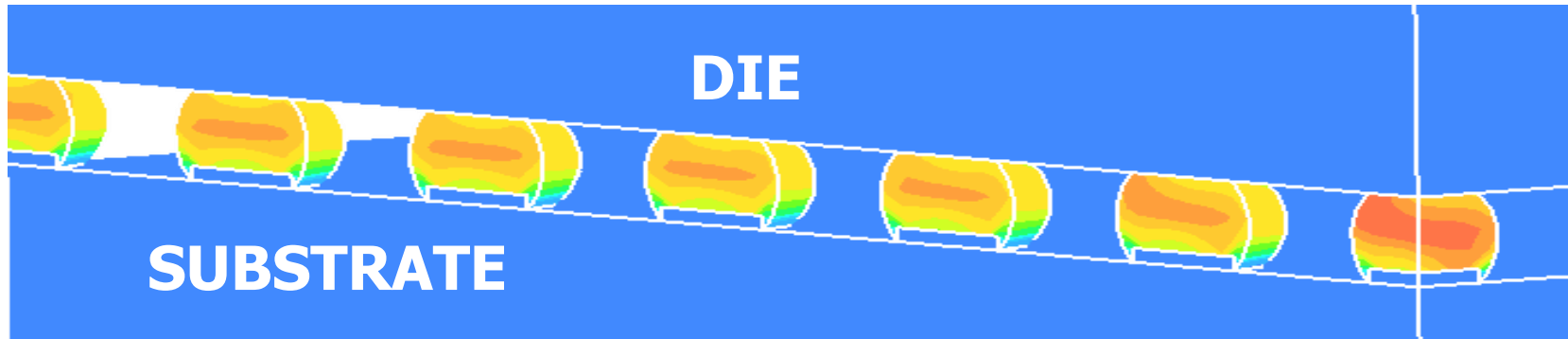
Identify Acceleration Factors



Reliability Predictions

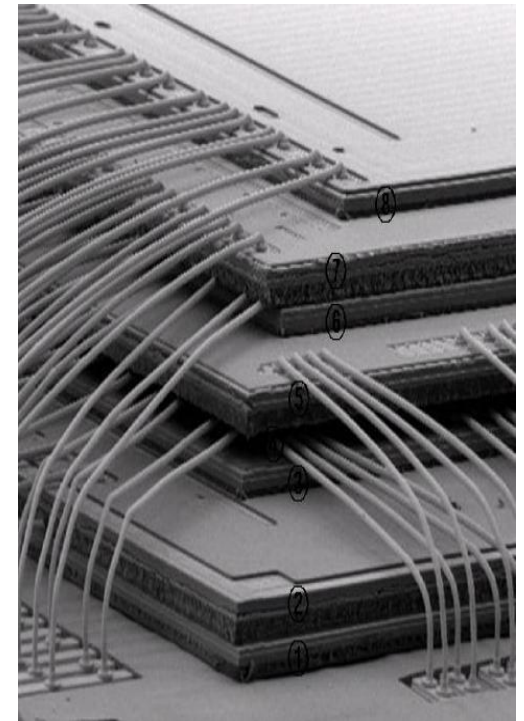


Design for Reliability



Content

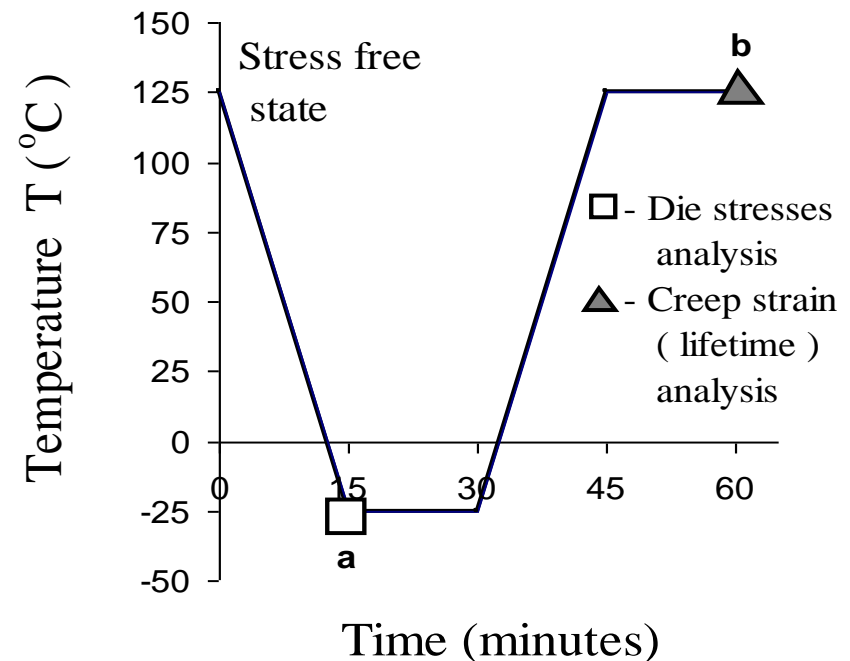
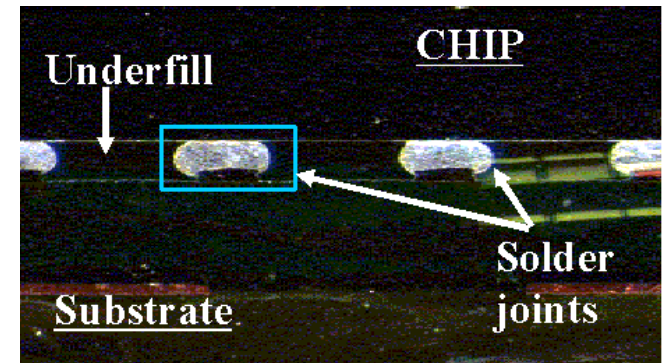
- What is System in Package (SiP)
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Flip-Chip Reliability

- Thermal Cycling
- CTE Miss-match
- Optimise Process conditions
 - Solder Joint Fatigue
 - Stress in the Die
- Design parameters
 - Underfill Young's Modulus (E)
 - Underfill CTE (CTE)
 - Stand-off height (SOH)
 - Substrate thickness (ST)

VIRTUAL DOE

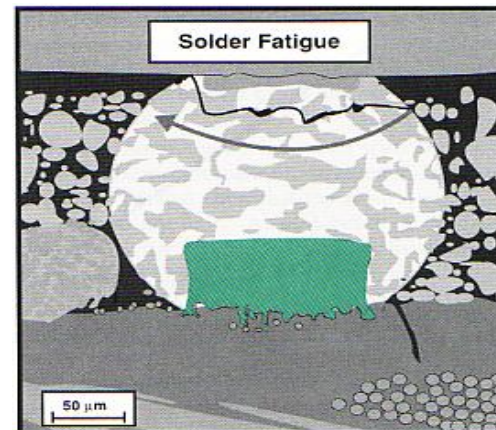


Capturing the Physics

- Large Strain Analysis
- Thermo-mechanical
- Materials
 - Elastic
 - Creep in Solder
- Failure mechanism
 - Solder Joint Fatigue
- Damage Model
 - Function of Strain Energy



Modelling part



Flip Chip Reliability

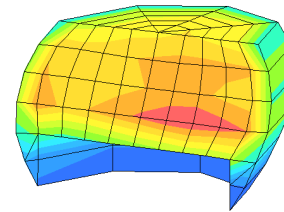
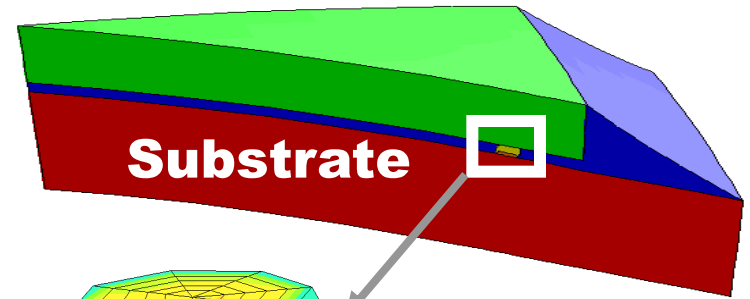
- Maximise lifetime
(Min Creep Strain)

- Subject to

Die Stress Constraint

$$\sigma^{Die} < 150$$

and specified limits for design variables:

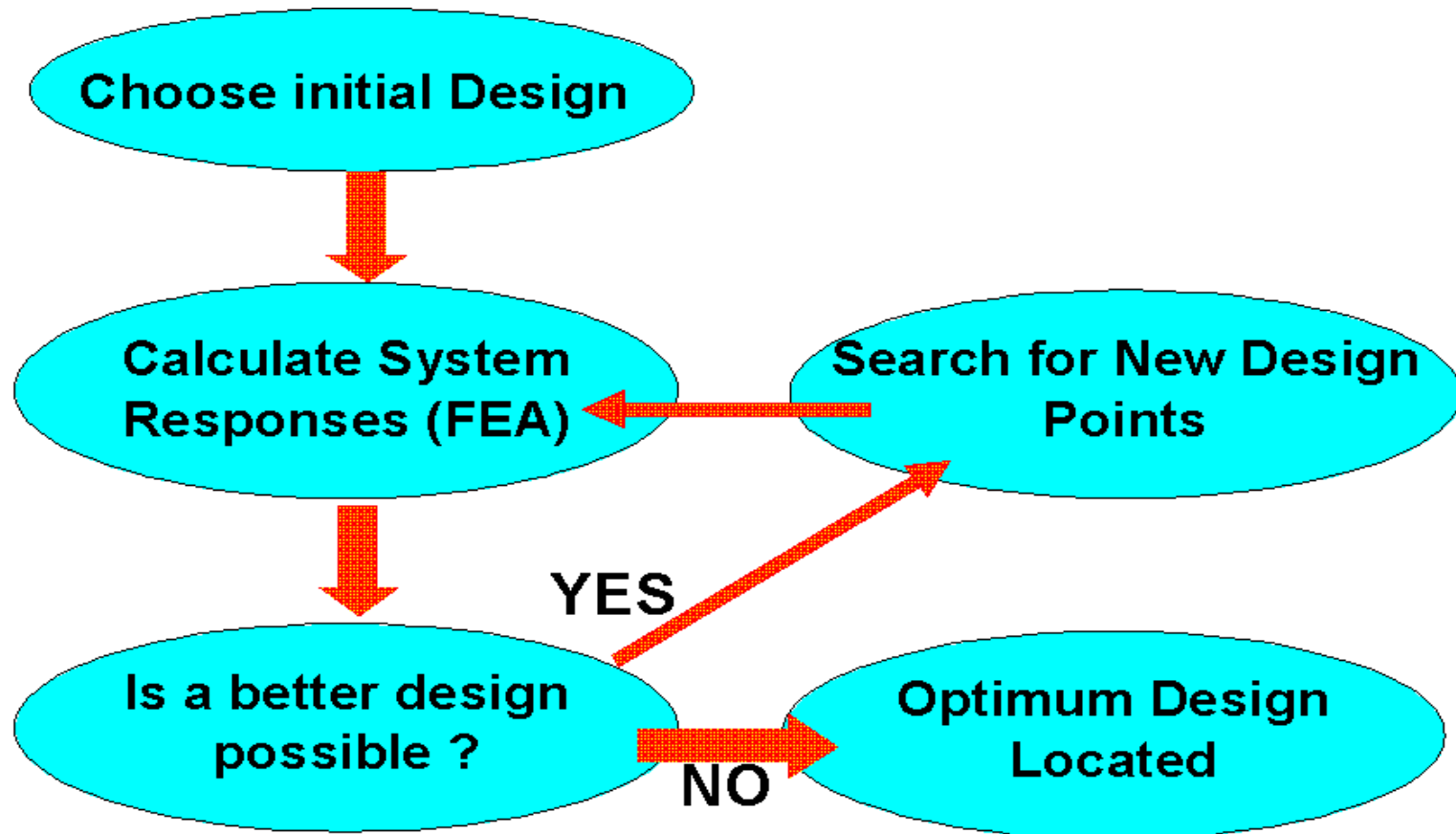


Fatigue failure under thermal cycling

Design parameters		Lower bound	Upper bound	INITIAL design	
1.	E of underfill (GPa)	2.0	5.0	3.0	
2.	CTE of underfill (ppm)	50.0	90.0	80.0	
3.	Stand-off height (μm)	104.0	156.0	130.0	
4.	Substrate thickness (mm)	1.2	1.8	1.5	

Optimisation Strategy

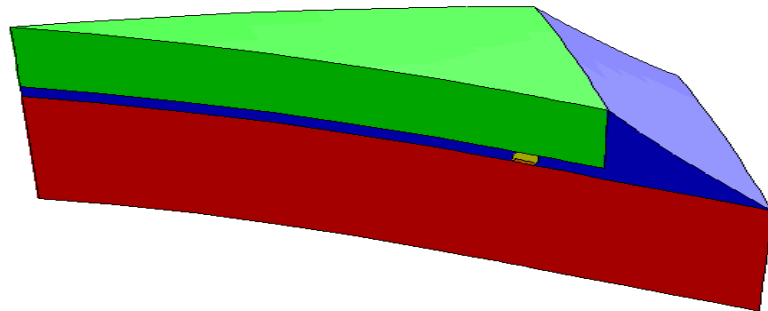
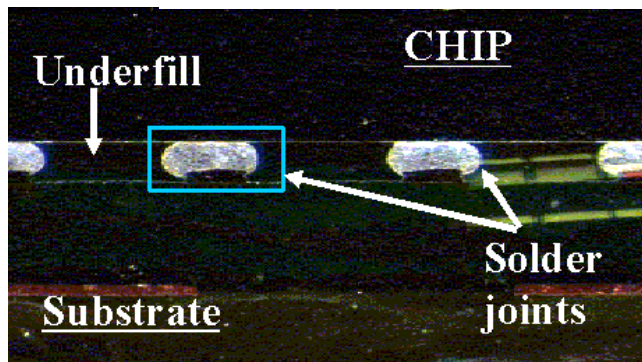
- Direct Gradient Approach
 - Modified Method of Feasible Directions



Results

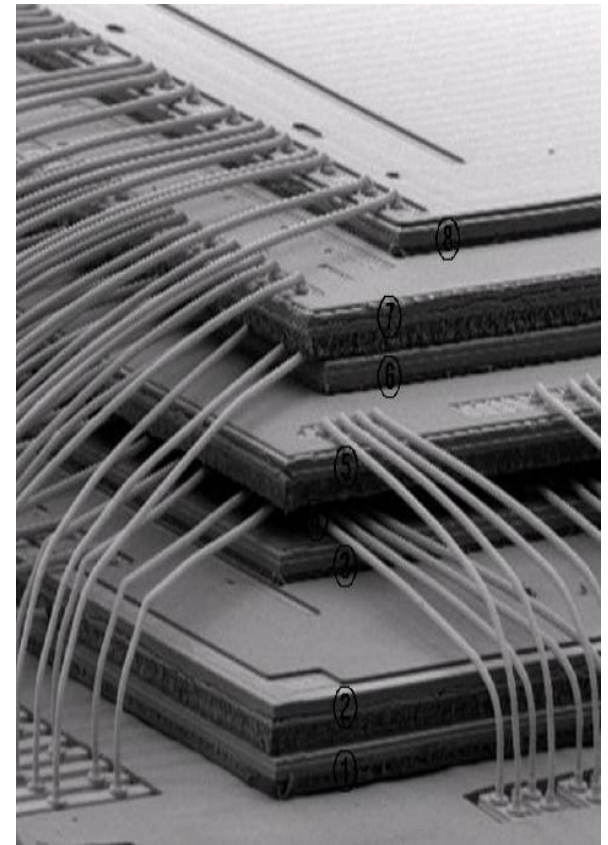
- Cycles to Failure increased from 136 to 589
- Stress in Die below 155MPa (constraint limit)

Design variables	Lower bound	Upper bound	Initial design	Optimal design
<i>Underfill Modulus</i> (GPa)	2.0	5.0	3.0	5.0
<i>Underfill CTE</i> (ppm)	50.0	90.0	80.0	50.0
Stand Off Height (μm)	104.0	156.0	130.0	156.0
Substrate Thickness (mm)	1.2	1.8	1.5	1.2
Constraint (Von Mises Die Stress [MPa])			119.62	133.41
Objective (<i>Cycles to Failure</i>)			136	589
Total number of FE analyses to obtain solution				15



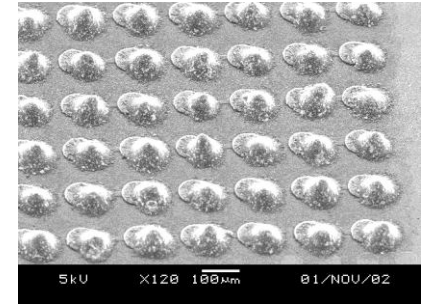
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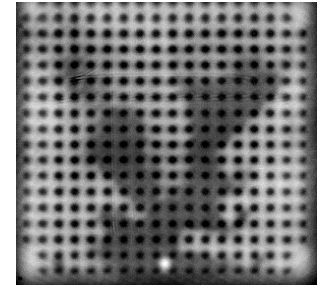
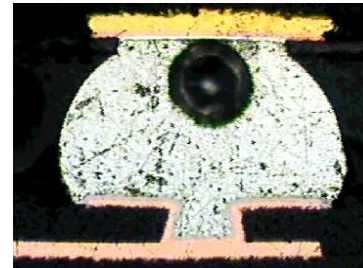
Design for Manufacture

- Poor quality in manufacturing can result in unreliable products



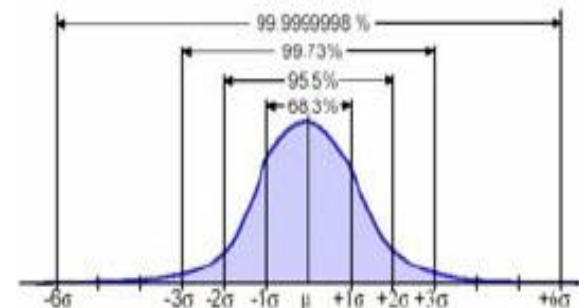
- Quality Control

- Integral part of Reliability:
- TQM; SPC; Six-Sigma, etc....

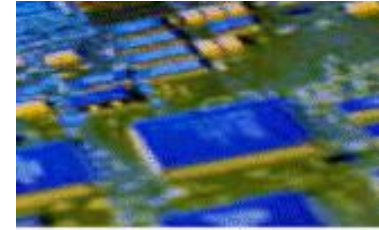
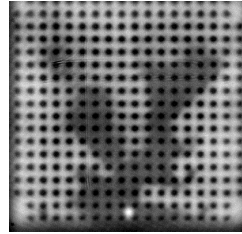
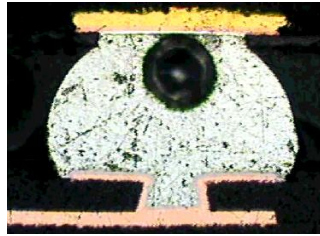
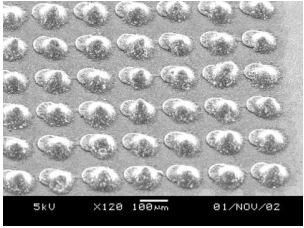


- Process Models

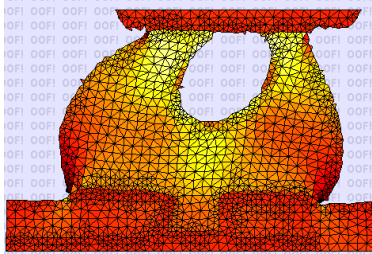
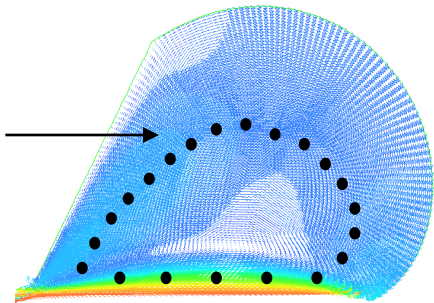
- aid quality control
- Identify process capabilities
- impact of small variations



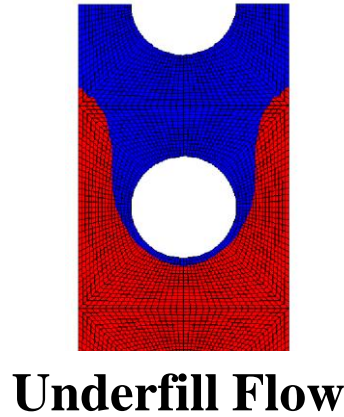
A lot can go wrong in Manufacturing



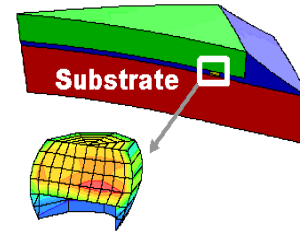
Solder Paste Flow



Reflow

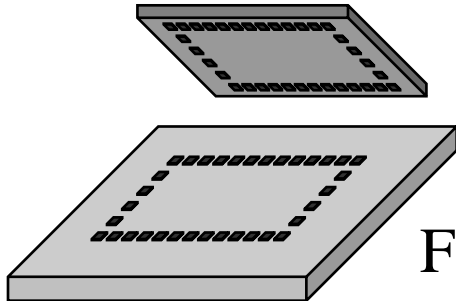
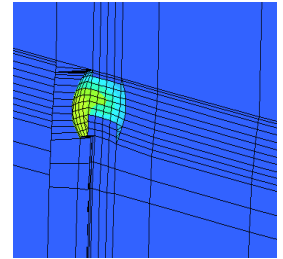


Underfill Flow

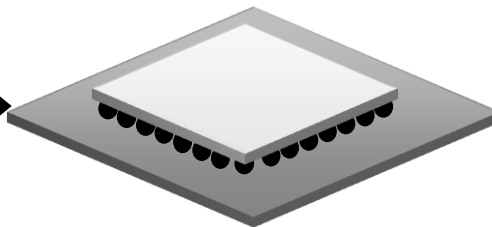


Cure

Thermal Cycling

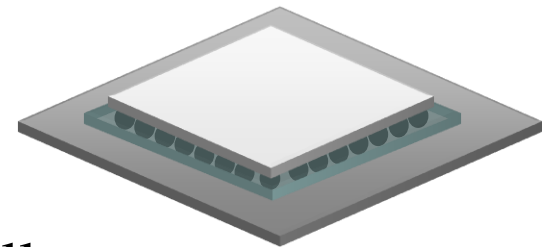


Furnace



Solder Solidifies

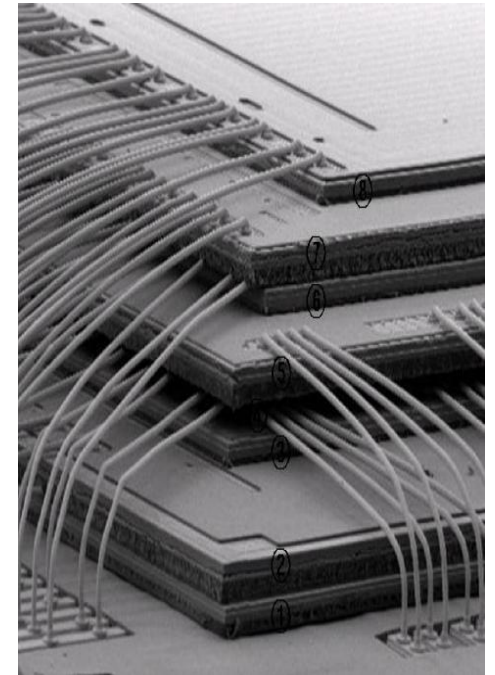
Apply Underfill



Final Product

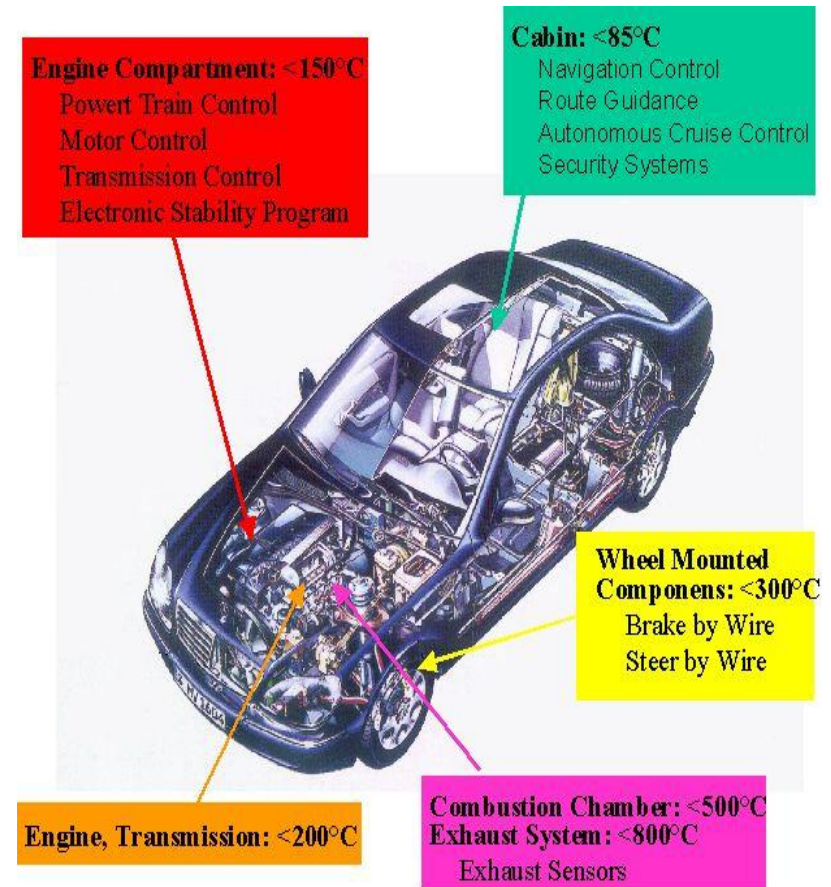
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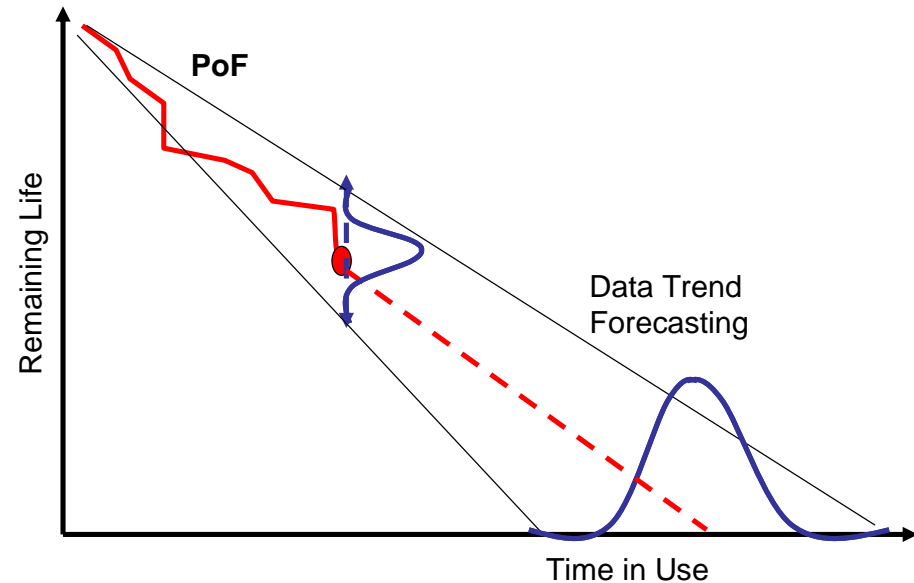
Why Prognostics

- Environmental Loads – Complex
- Failure may occur earlier or later than expected
- Prognostics
 - Early warnings
 - Effective Maintenance
 - Health management



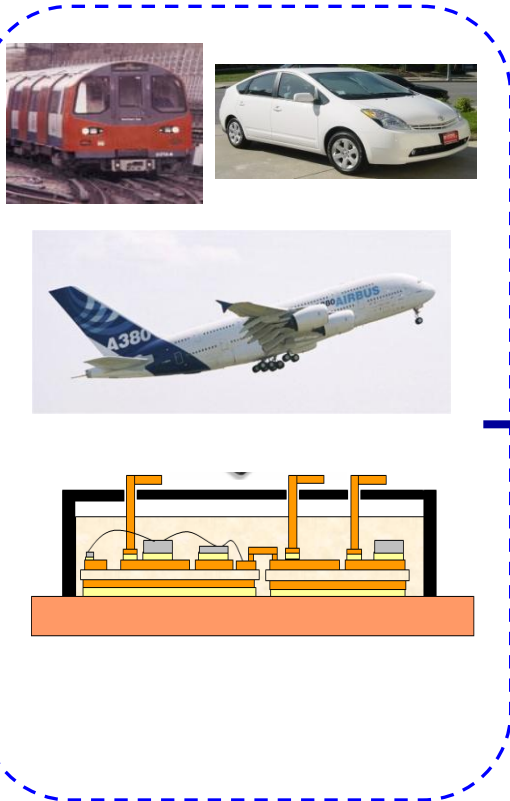
Modelling for Prognostics

- Data Trend Analysis
 - Identify changes in Electrical Performance
 - Diagnostics
- Physics of Failure
 - Reduced order models
 - Predicts remaining life
 - Accuracy of PoF models?
- Integrated Approach
 - Bayesian Networks
 - Statistical Approach
 - Updates PoF models based on new data

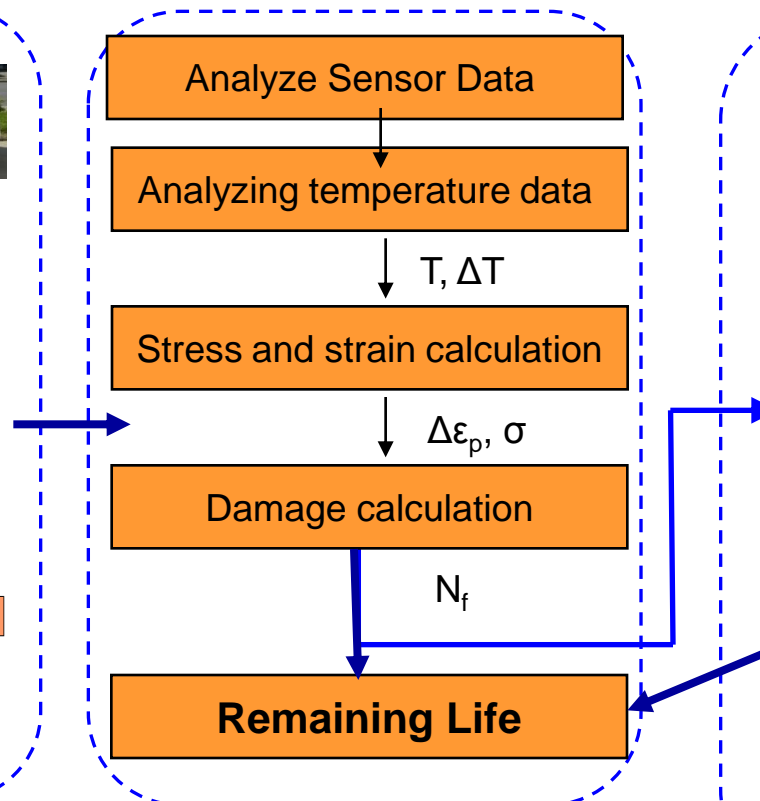


Modelling for Prognostics

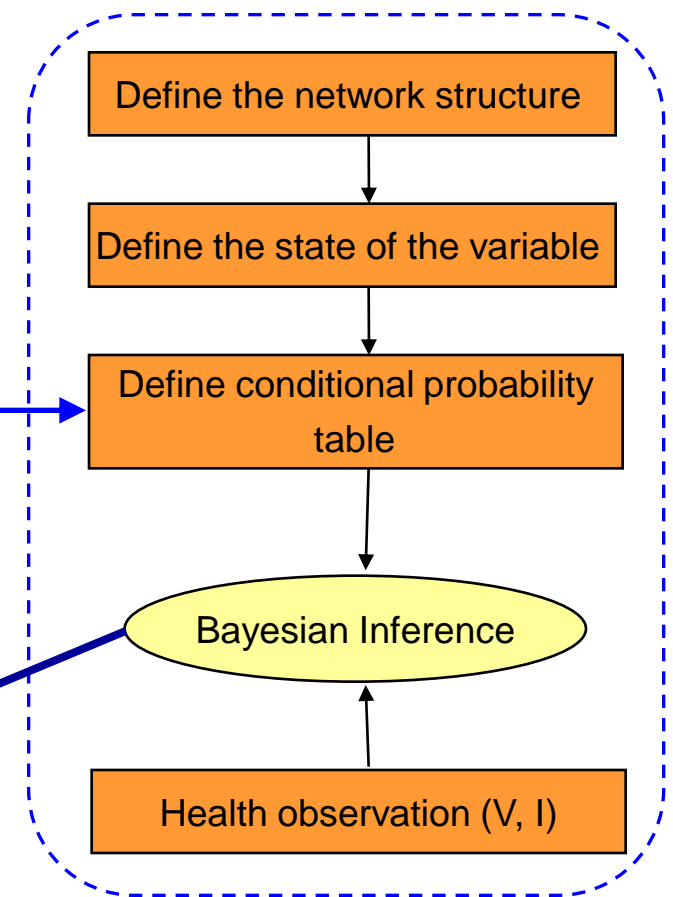
Sensor Data



Physics of Failure Models



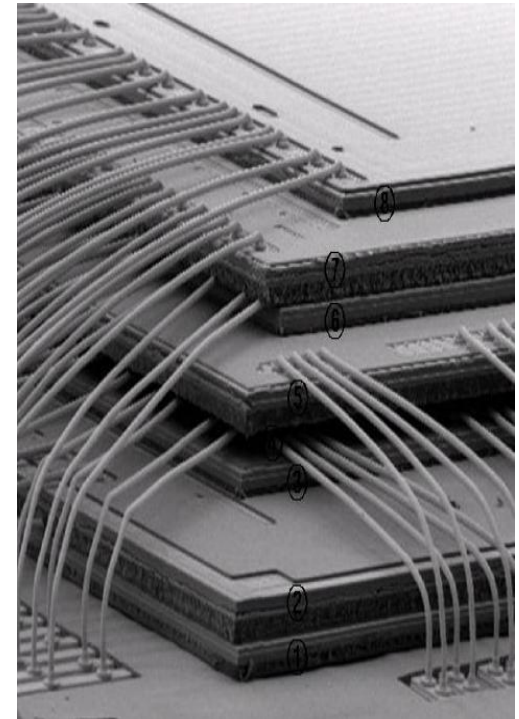
Bayesian Network



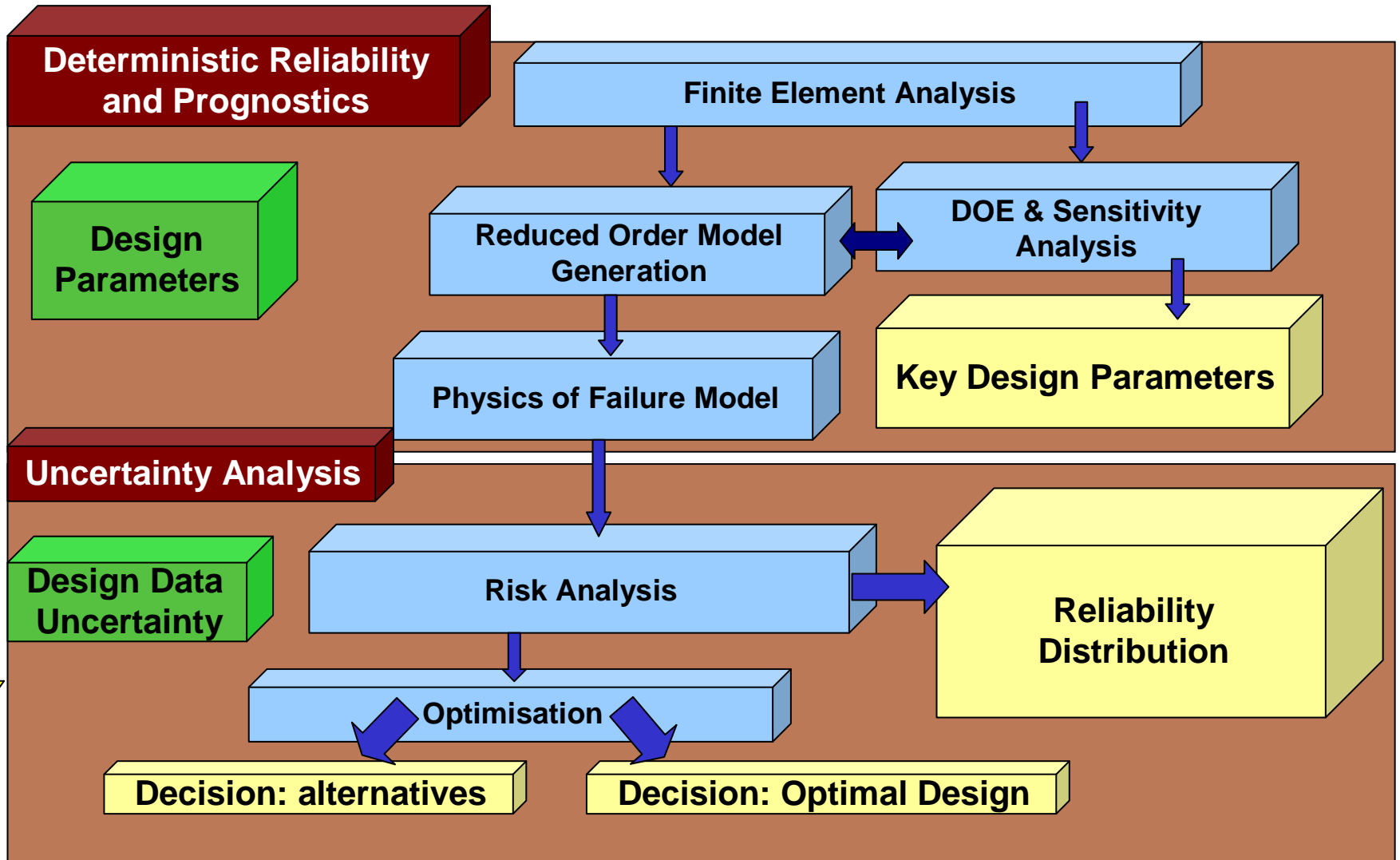
Methodology being developed for Power Modules

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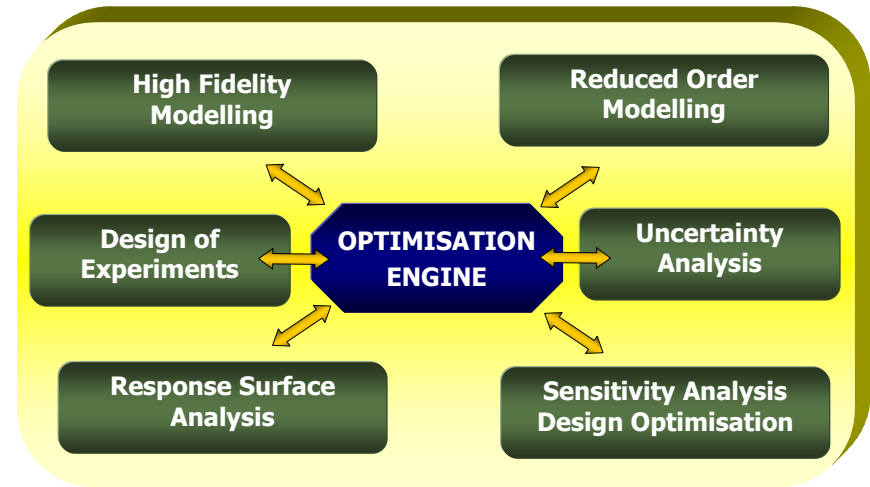


Quality informed Reliability



Future Challenges

- Materials Data
- Failure Models
 - Through Silicon Via
 - Solders....
- Reduced Order Models
 - Manufacturing
 - Performance
 - Reliability
 - Prognostics
- Integrated DFX
 - Manufacturing
 - Reliability



ROMARA TOOL (Greenwich)

