

Conclusions

- Complex Assemblies with numerous potential failure + degradations mechanisms poorly understood
 - Expensive test process
 - Hardware bugs – random particles
 - What DfT / Test Support / Health Monitoring to build into the SiP?
 - Will we need embedded test software – eg. Statistical processing
- Split between design test and verification and package / assembly & integration test / verification : new solutions to verify connectivity between components – boundary scan not sufficient. Test complexity a function of process maturity, test access to sensors, electronics etc? what can be reused from the SoC / Board test area – what is specific to SiP? Signature testing? Characterisation test very different WRT production test
- Physics of Failure / ROM / Tools support : some FEA support, split between engineers in use of simulation – important for simulation experts to liaise with designers / technologists – but ultimate goal is more reliability simulation up-front
- Extension to prognostics, fault tolerance and self-repair? Application dependant automotive & health? Need for redundancy, self-test important
- Test access architecture for SiP test?
- Exploitation of the test community (eg. On-chip resource reuse) : needed – why re-invent the wheel, dialogue on specific products – move from abstract level
- Questions
 - Are these issues appropriate for dedicated focus (ie. workshop) : universities not very active, ETS wants to be on the leading edge, where will the delegates come from? Definition of a SiP? Need to be more application focus, maybe a SiP session in ETS?
 - If so how to move forward, if not which community will address? Maybe Comms, MicoMachine Summit, IMSTW, target dedicated MEMS test engineers?
 - Where are the Grand Challenges? What will industry do? What should be done collaboratively? Packaging, Enabler of SiP is integration, Wireless testing