Reliability & Test Engineering on PICS based SiP

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Outline

- IeMRC System-in-Package Projects
- Partner Profiles
- Introduction to SiP and Challenges (NXP example)
- IeMRC Research
  - Introduction to reliability modelling (extended by Stoyan)
  - Health Monitoring & Embedded Test

Project Statistics

- **Design for Manufacture Methodology for SiP**
  - Academic partners : Lancaster University & Greenwich
  - Industrial partners : NXP, Flowmerics, Coventor & Selex
  - £206K – Nov 2005 – Nov 2007
  - Focus : Reliability Engineering of SiP assemblies
- **Integrated Health Monitoring of MNT Enabled Integrated Systems "I-Health"**
  - Academic partners : Lancaster University & Heriot Watt University
  - Industrial partners : NXP, QinetiQ, Coventor, MCE
  - Focus : Embedded Test & Health Monitoring of SiP based systems

SiP-Design

- **Design for Manufacture Methodology for SiP**
  - Realise algorithms and associated code to generate an integral thermal map across a behavioural model of an SiP structure.
  - Realise algorithms and associated code to model and couple electromagnetic and electrostatic fields into functional devices and materials within an SiP structure.
  - Realise a method of injecting defects and degradation into structural SiP models. Address the test issue.
  - Demonstrate the above advances in an industrial virtual prototype environment

“I-Health” project SP/05/01/03

- **Integrated Health Monitoring of MNT Enabled Integrated Systems**
  - The potential to realise low cost temperature, stress, humidity and EM field sensors for integration in a health monitoring architecture.
  - Electrical only strategies that requires low performance electronics to monitor non-electrical functions both on-line and in production.
  - A solution for embedding both sensing and electrical monitoring functions within a SiP level test access and control architecture together with decision making functions based on re-use and / or reconfiguration of existing functions and both fault tolerance and self-repair through redundancy and emulation.
  - Implementation solutions including on-chip, on-substrate and through dedicated low cost health inserts for both silicon and LTCC platforms.

Lancaster University

- **Centre for Microsystems Engineering**
  - **4 academic staff, 5 RA’s, 4 PhD’s**
  - **Delivered against £3.4M in grant income over the past 10 years**
  - **Leads the European Design for Micro & Nano Manufacture community through the FP6 Network of Excellence (PATENT-DfMM)**




What is System-in-Package, or SiP?

- The integration of several integrated circuits and components of various technologies (RF, analogue, digital, in Si, in GaAs) in a single package, resulting in one or several electronic systems
- Related key words:
  - Heterogeneous Integration, System-on-Chip, SoP

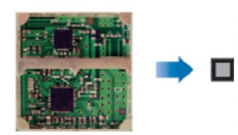
Stacked Structures

Side-by-Side Structures

Embedded Structures

SiP key drivers and benefits

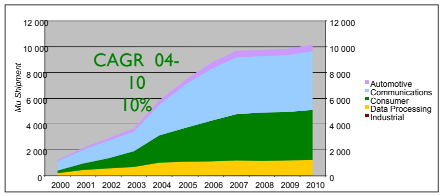
- Size reduction
- Functional performance improvement
- Combination of several functions
- Cost reduction
- Speed-to-market due to the reuse of existing ICs
- Complete system integration



Market Trends : Industry moves to SiP

- **Gartner updates its SiP Market Projection every quarter**
- **Gartner view of the market has changed since 3Q 04 with 10% CAGR 04-09 compared to 5% CAGR 04-09 for Semiconductors**

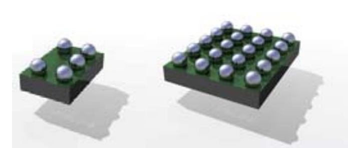
SiP Market Projection

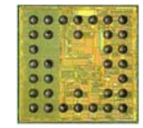


Source: Gartner 1Q06

- **Gartner sees as much SiP in Consumer as in Communication**

Wafer-Level Chip-Scale Packaging: existing NXP Products





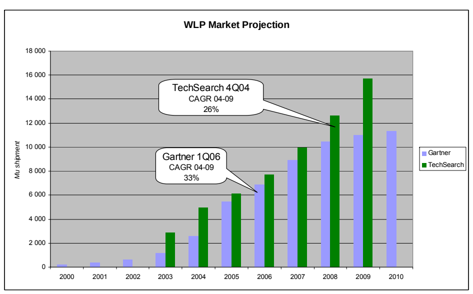
- Integrated Discretes (ESD protection + EMI filtering)
- No redistribution layer (RDL) needed: direct bump on IO.

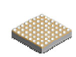
- **FM radio (2005)**
- **RDL needed (higher cost than direct bump on IO)**

- Still few product lines
- Qualified circuits < 12mm²

- Questions:
  - Extendibility to larger circuits?
  - Applicability to more product lines?

Market Trends : Industry moves to WLP





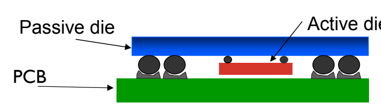
- Expected CAGR 04-09 > 25%

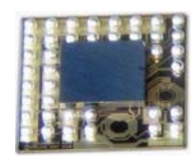
Source: Gartner 1Q06 + TechSearch 3Q04

- Both TechSearch and Gartner confirms a significant growth of WLP deliveries
- 70% of WLP applied to Integrated Passives in 2005

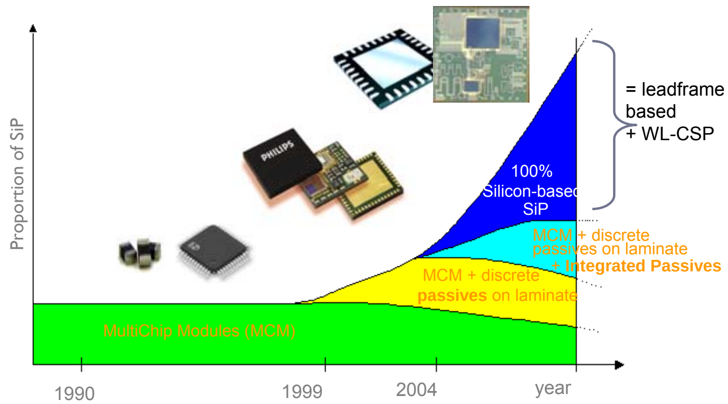
Wafer Level SiP

- WL-CSP and SiP are motivated by identical drivers:
  - Size reduction
  - Performance enhancement
  - Cost reduction
- WL-CSP largely applies to integrated passives. SiP will use passive substrates able to house a wider device range – eg. MEMS
- They will merge into WL-SiP (NXP patents)

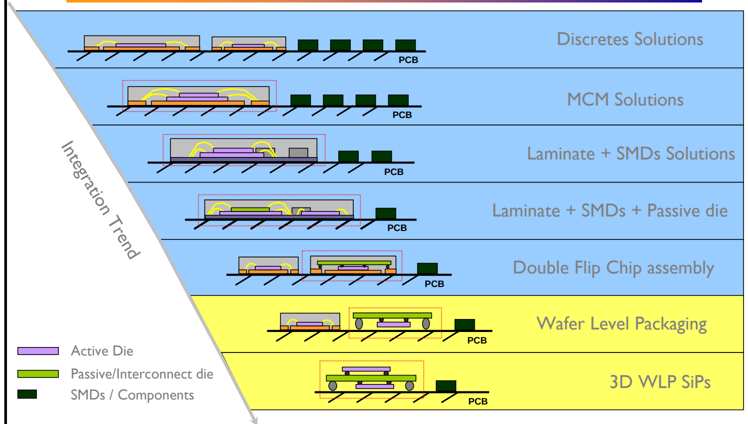




Move to full silicon-based SiPs

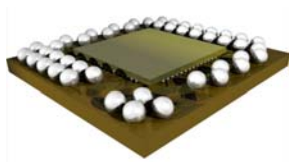


NXP SiP Platforms Trend



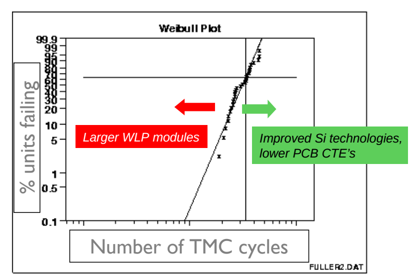
WL-SiP: challenges

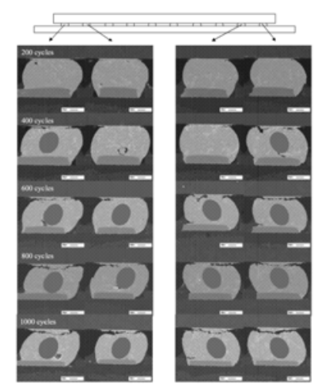
- Larger WL-CSP modules (because SiP are larger than current WL-CSP parts)
  - Board Level Reliability (solder fatigue issue)
- Assembly flow
  - Final Test
  - Marking
  - Packing
  - Storing
- Customer acceptance
  - Customers and assemblers (pick & place, under fill dispensing on PCB)
  - Designers (sockets for evaluation boards)
  - PCB makers: downwards CTE curve to be supported



Board Level Reliability: solder fatigue (1)

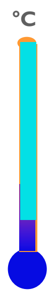
- Visible by thermal cycling





Board Level Reliability : solder fatigue (2)

	Si	FR4
CTE (ppm/K) Coefficient of Thermal Expansion	3.5	16

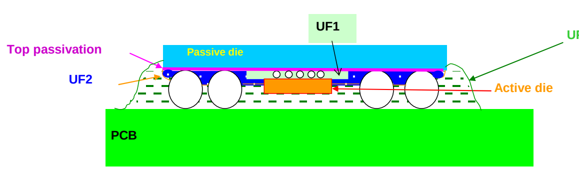


- Difference with BGA: BGA is a FR4/FR4 stack. Differences of CTE to be considered only between substrates and bumps

Simulation and Modelling Requirements

- Accurate simulation and modelling is useful
  - In the short term
    - To assess reliability of current WL-CSP technologies with respect to larger sizes
    - To compare possible technology options
      - New materials (underfills, bump alloys, PCB's)
      - New balling layout rules
  - In the longer term
    - To "virtually qualify" WL-CSP parts:
      - How to make sure a new product has every chance to first time pass qualification stresses according to the company specific General Quality System?

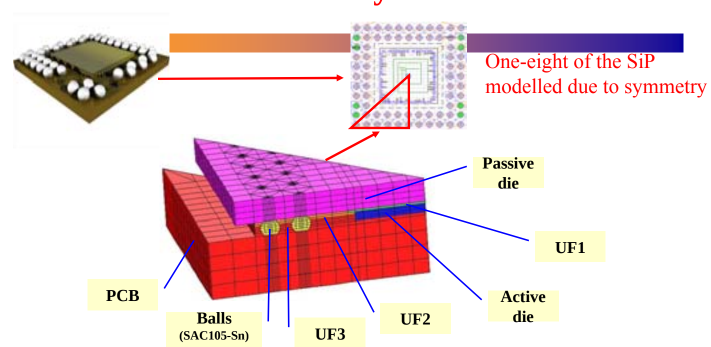
IeMRC Research



Technology focus

- To date around the NXP platform
- Address reliability issues today and integration trends in the future

Reliability Studies



SiP Parameters:

- Sizes (number of balls in a row): **11×11**, **9×9**, **7×7**
- Passive Die Thickness : **L** - 200µm or **H** - 400µm
- UF2 (reinforcement) present: **R**
- UF3 present: **U**
- Neither UF3 nor Reinforcement is present: **N**

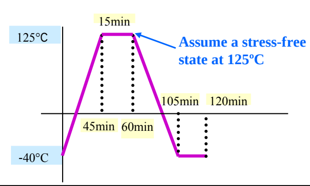
Plan of Experiments

Test	Size	UF	Passive die thickness
11HR	11×11	UF2	400
11LR	11×11	UF2	200
11HU	11×11	UF3	400
11LU	11×11	UF3	200
11HN	11×11	None	400
11LN	11×11	None	200

Test	Size	UF	Passive die
09HR	9×9	UF2	400
09LR	9×9	UF2	200
09HU	9×9	UF3	400
09LU	9×9	UF3	200
09HN	9×9	None	400
09LN	9×9	None	200

Test	Size	UF	Passive die thickness
07HR	7×7	UF2	400
07LR	7×7	UF2	200
07HU	7×7	UF3	400
07LU	7×7	UF3	200
07HN	7×7	None	400
07LN	7×7	None	200

Thermal Cycling Profile



Simulation Set Up

- **Inelastic material behaviour of solder (Creep Rate Equation);**

$$\dot{\varepsilon}^{creep} = A\left[\sinh(a\sigma)\right]^n \exp\left(\frac{-Q}{RT}\right)$$

- **Simulation response of interest –accumulated creep energy density per cycle:**

$$W_p = \sum_{\Delta t} \frac{\sum_{i=1}^{N} \int_{V_i} \sigma(\Delta\varepsilon^{creep})\, dV}{\sum_{i=1}^{N} \int_{V_i} dV}$$

Δt – time steps
N – number of elements
V_i – volume of i-th element
σ – stress vector
$\Delta\varepsilon^{creep}$ – vector of creep strain increment for Δt

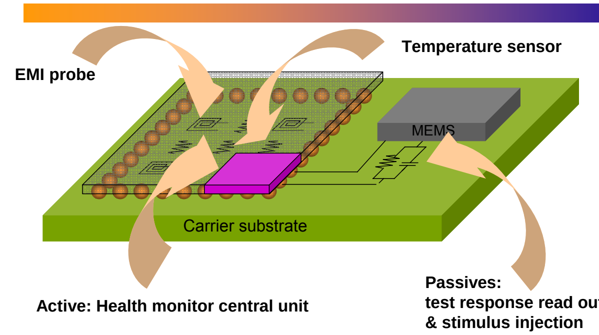
- **Life prediction model (for SnAgCu) – uses FEA predictions for damage *Wp* and relates to cycles to failure:**

$$N_f = (0.0014 W_p)^{-1}$$

Conclusions

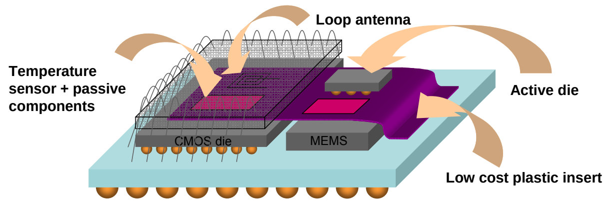
- The presence of UF3 can improve reliability of the Stacked SiP Package
- SiP design parameters
  - SiP size and presence of UF3 are the most influential parameters
  - Passive Die thickness and presence of UF2 have less significant effect on solder joint reliability
  - **Recommendation**: to improve reliability ⇨ smaller package size with suitable UF3 and thinner Passive Die

Health Monitoring – embedded concept



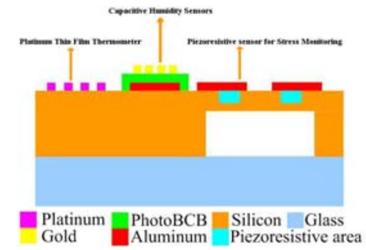
- Integrated sensors: temperature, EMI probes etc…
- MEMS testing
- System reconfiguration

Health Monitor – Insert Concept



- Possibility for stacked SiP
- Standard pin-out / foot print for test interface?
- Dependent on advances in polymer electronics

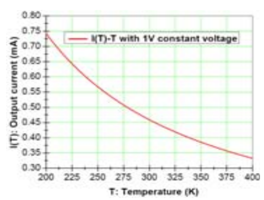
Monitoring the Package Environment

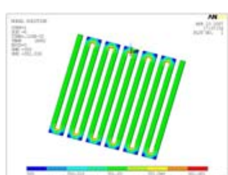


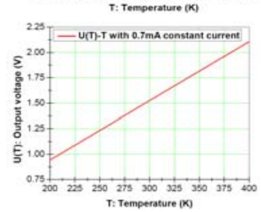
- A schematic of an integrated multi-sensor chip for condition monitoring in MNT enabled systems, e.g. the SiP based microsystems, comprising:
  - A thin film resistance temperature sensor
  - A capacitive humidity sensor based on the oxidised photosensitive BCB polymer with enhanced sensitivity and response time
  - A piezoresistive MEMS sensor based on micromachined polysilicon film for pressure/stress monitoring.
  - A microsensor for monitoring of electromagnetic radiation may also be integrated within the sensor chip/platform

Platinum Thin Film Resistance Thermometer

- The thin film resistance thermometer:
  - Temperature range: -200ºC ~ 1000ºC
  - Advantages: Accurate, stable.
  - Disadvantages: Self-heating, nonlinear response.

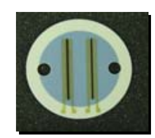


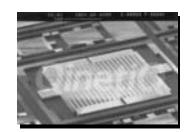




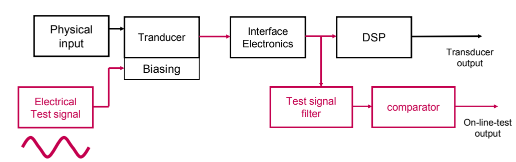
Non-electrical functions – bias superposition

- Electrical only test & monitoring techniques for MNT systems





✓ Feasibility on magnetometer, accelerometer, conductance sensor

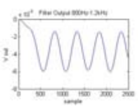


Is it possible to use this method as a generic method to test MEMS structures?

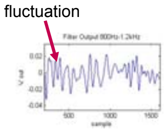
Implementation – embedded accelerometers

Test output is unstable under acceleration conditions – on-line applicability??

Demonstrator board with QinetiQ accelerometer



Test output with no acceleration

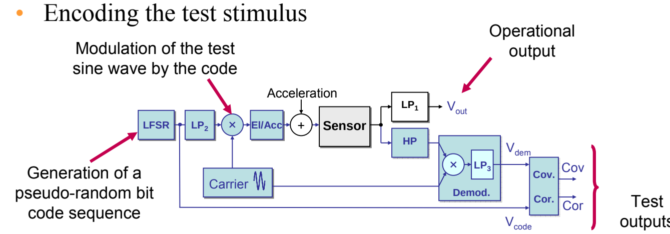


Test output with 10g acceleration @ 100Hz

- Step 1: Identify the causes of the fluctuation
- Step 2: Develop solutions to solve the issue of the test output fluctuation
- Step 3: Evaluate the fault coverage capability using fault simulation

Solution – encoding of test stimuli

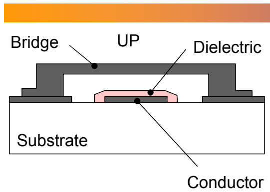
- Encoding the test stimulus



Novel architecture

- A pseudo-random code sequence modulates the test sine wave
- The code is retrieved by demodulation at the output
- Covariance and correlation algorithms are applied
- The covariance gives a value related to the sensor sensitivity
- The correlation gives information on the integrity of the covariance

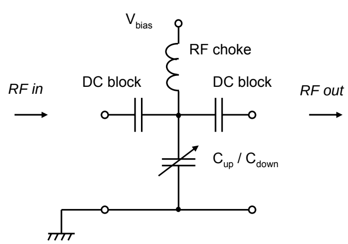
Application to RF MEMS switch



Raytheon/TI* switch:

Cup = 35fF
(Insertion loss@10GHz = 0.025 dB)

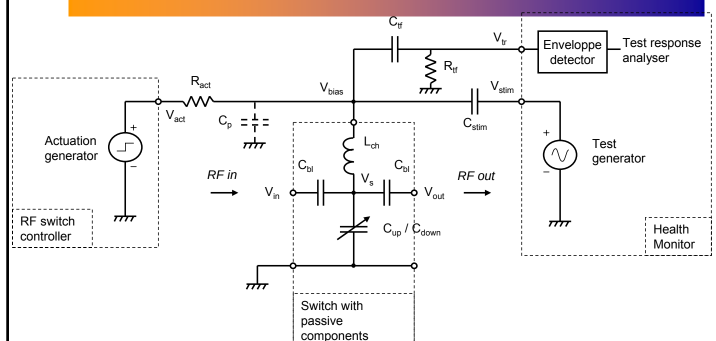
Cdown = 3.5pF
(Isolation@10GHz = 15 dB)



Switch model with the biasing circuitry in a shunt configuration

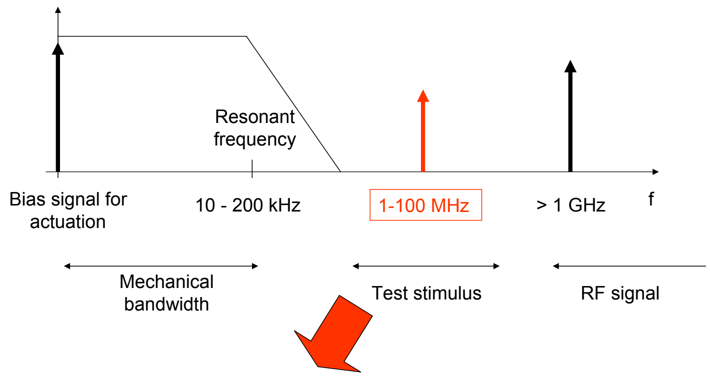
*Raytheon/TI switch

Test implementation strategy



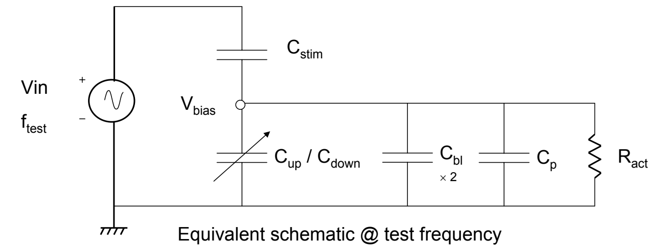
Passive components integrated on the substrate

Test signal frequency



✓ **Relatively low frequency**

Limitations of the test technique



Equivalent schematic @ test frequency

- C_{bl} – DC block capacitor: $C_{bl} > 3pF$ for $IL(C_{bl}) < IL(C_{up})$
- C_p – Stray capacitance of the biasing line: $C_p < 1pF$
- R_{act} – In series resistor on the biasing line to prevent a short: $R_{act} > 450\Omega$ for $IL(R_{act}) < IL(C_{up})$

The limiting factor is the capacitance of the DC block

Conclusions

- Work to date focused around silicon based WL-SiP
  - Embedded health monitoring
  - Strategies for non-electrical functions
  - Reliability simulation – structure & assembly
    - Impact of underfill on solder reliability
    - Impact of moulding process
    - Impact of fan-out
    - Analytical reliability prediction strategies developed
  - Extend to SoP – eg. Ceramic based
  - Investigate integration into EDA tools