



The Future of Embedded Test within the Design for Micro & Nano Manufacture NoE

www.patent-dfmm.org

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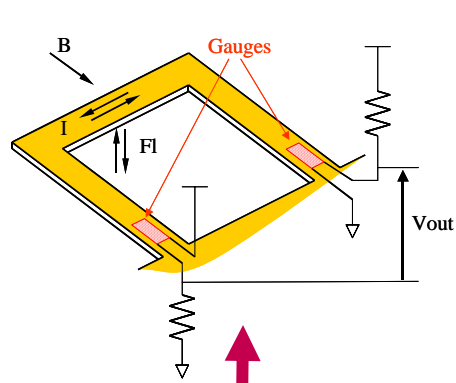
«Design for Micro & Nano Manufacture (NoE PATENT-DfMm)»
Network of Excellence funded by the European Commission (EC FP6: IST, Unit C2, Contract 507255)

- Embedded Test Partners
- Technical Background in Embedded Test
- Embedded Test Centre
- Activities within 2007 and post PATENT-DfMM

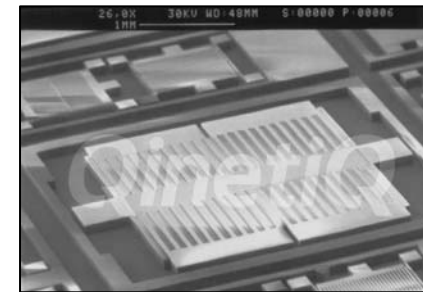
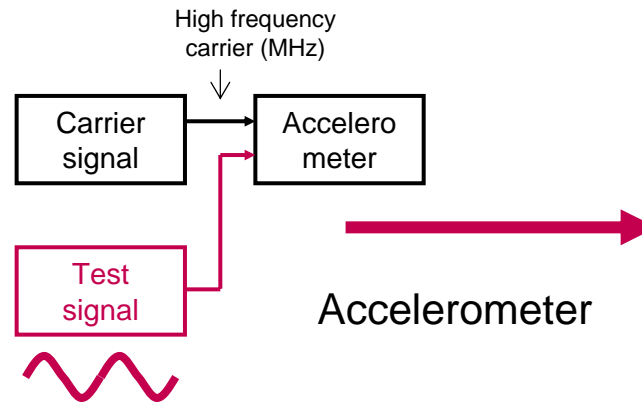


6 Organisations
25+ experts

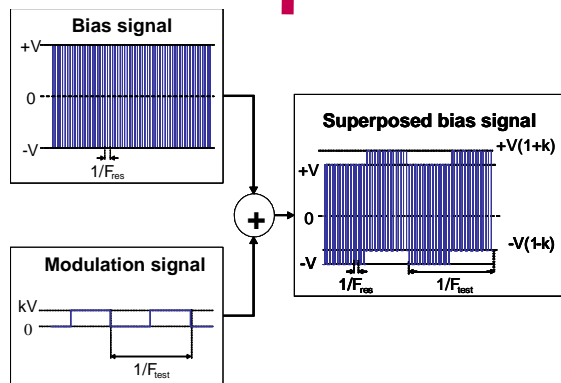




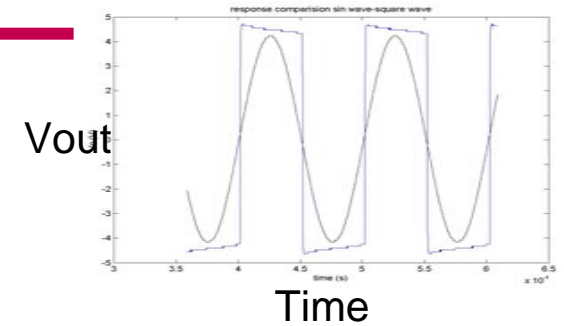
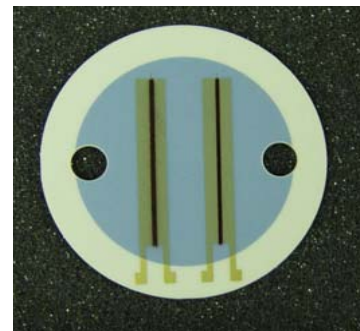
Magnometer

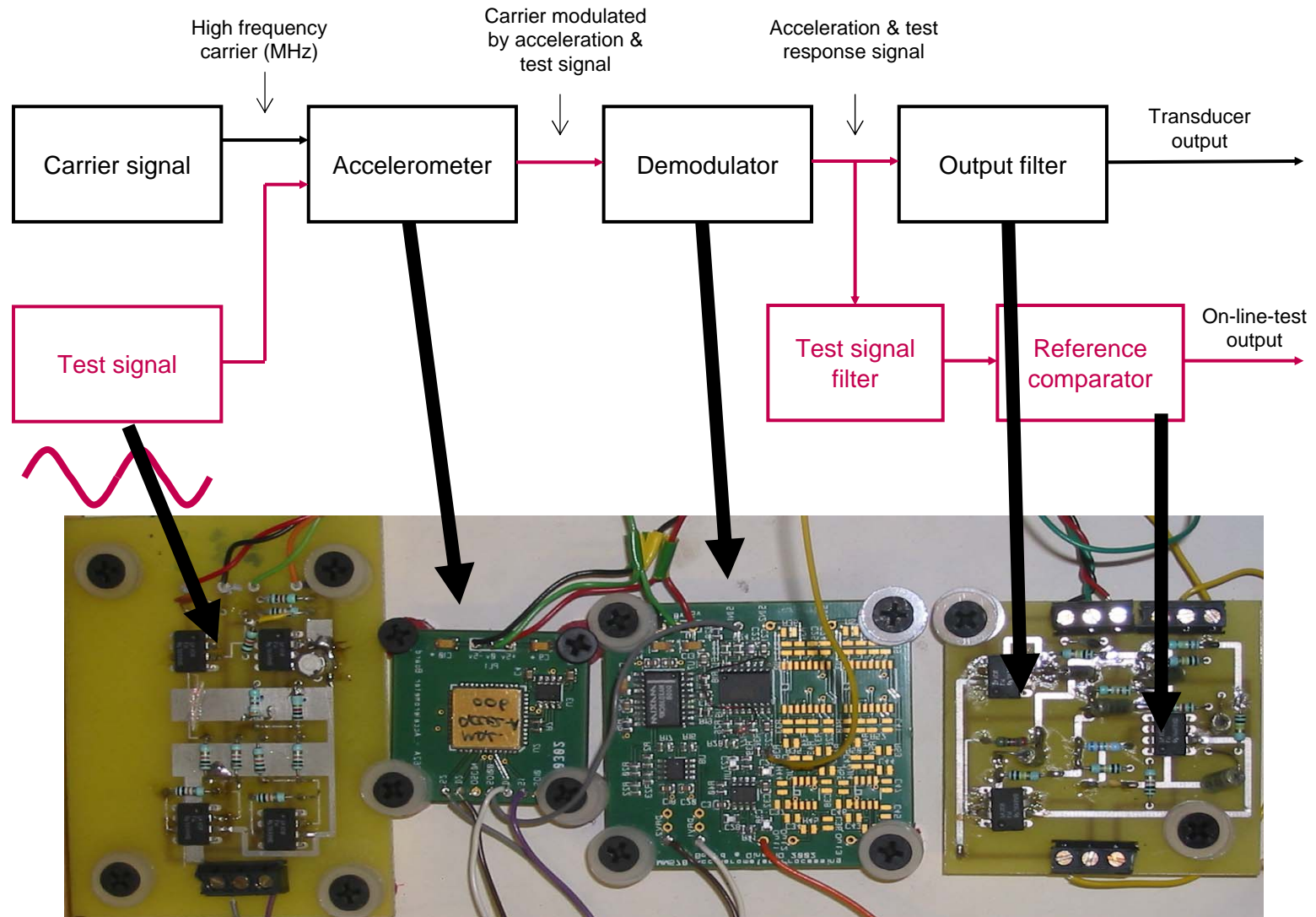


Accelerometer



Conductance Sensor



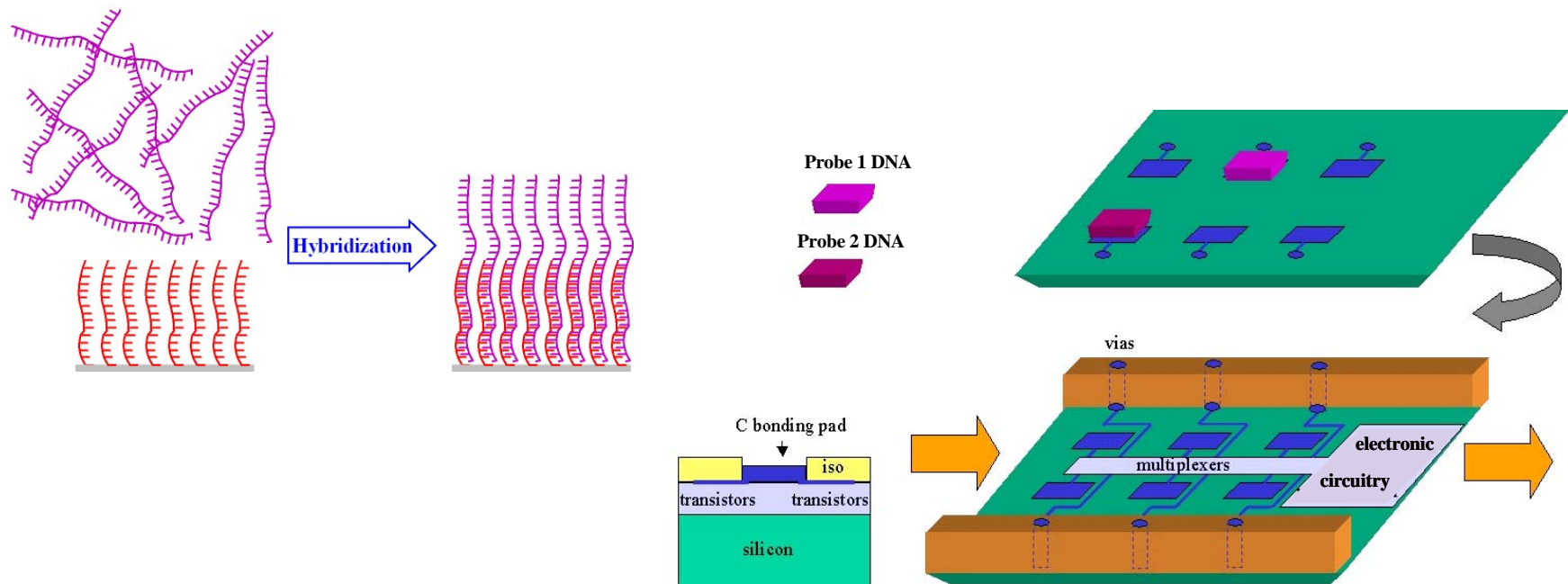




DfMM Demonstrator #2 Conclusions

- ❑ We have proved that it works
 - The test signal does not interfere with the sensor signal
 - The sensor signal does interfere with the test signal, but we can filter most of it out
 - Implementation using SMT components in a shielded box to provide a cleaner output
 - It is a go/no go test
- ❑ DSP techniques can be used provide a 'clean' test output
 - 10g testing!!!!!!!
 - Would require post processing
 - Verification would be delayed

- MESA+, ULAN, LIRMM
 - Can the testability and/or reliability of the detection process be improved through DfT?
- IMSTW 2005, IEEE Sensors conference

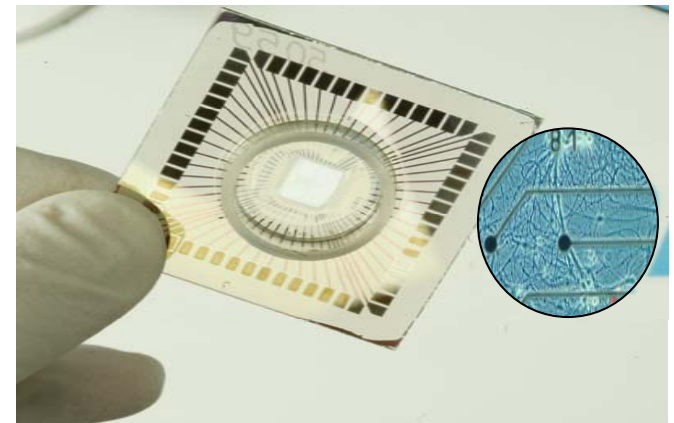


Integrated Testing of Bio-MEMS

H Liu & A Richardson (ULAN), Alan Brown & Dr Richard Heal (QinetiQ), Prof Hans Kerkhoff (MESA+) Dr Norbert Dumas (ULAN / LIRMM)

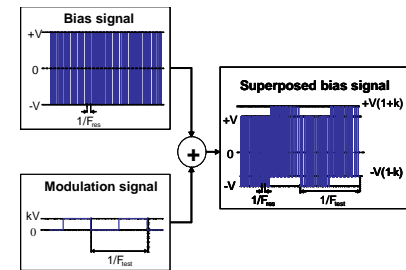
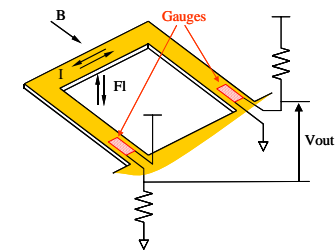
EU Framework 6 NoE "PATENT-DfMM" Phase 3 – Industrial demonstrator

There is great potential for using MNT to realise a range of microsystems for detection and manipulation of biological quantities. Reliability and testability of these systems however remains unstudied. This work will investigate methods of integrating built-in test and health monitoring functions into biological microsystems. Work will be initially focussed around the microelectrode array platform used to study the electrical activity of neuronal or cardiac cells. This commercially available platform is currently being developed as a screening method for drug safety pharmacology and would benefit enormously from inbuilt test and reliability systems.

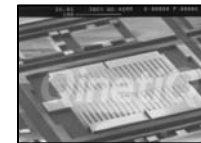


Micro-electrode array used to analyse the electrical activity of living cell (neuronal cells shown in inset – COURTESY OF QINETIQ).

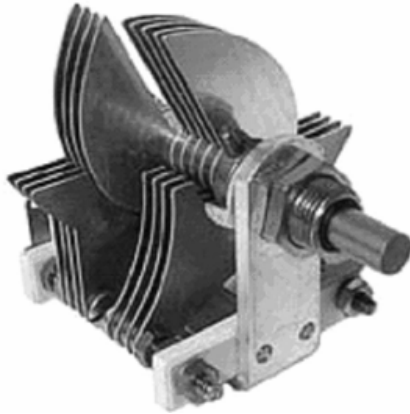
- ❑ Embedded electrical only test solutions for functions with non-electrical interfaces
- ❑ **A Cluster of experts :**
 - Lancaster University. CNRS, Montpellier, QinetiQ
- ❑ **Services :**
 - Feasibility studies on embedded test solutions for microsystems and system-in-package technology featuring functions with non-electrical interfaces
 - Access to extensive information database and consultancy
 - Design service for self-test or condition monitoring functions
 - Prototyping facility (silicon and board based)



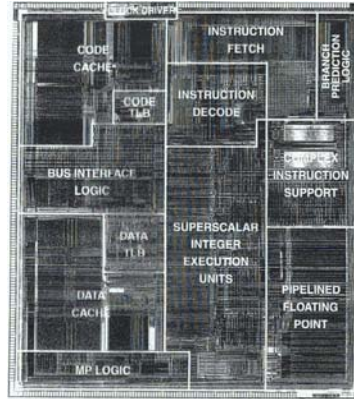
Injection of test signals into bias structures to test magnetometers



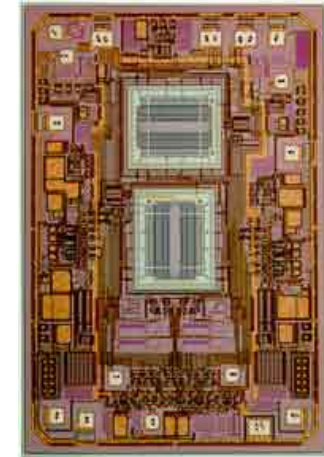
Prototype solution for accelerometers



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SiP, SoC, Hybrid

Manufacturing Costs

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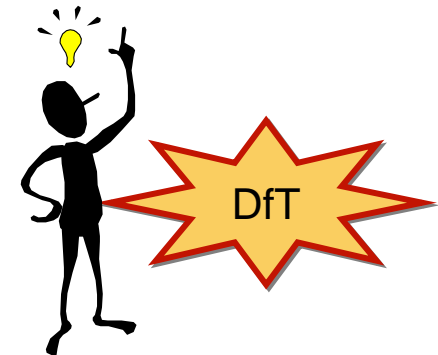
Manufacturing Test Costs (Go/NoGo)

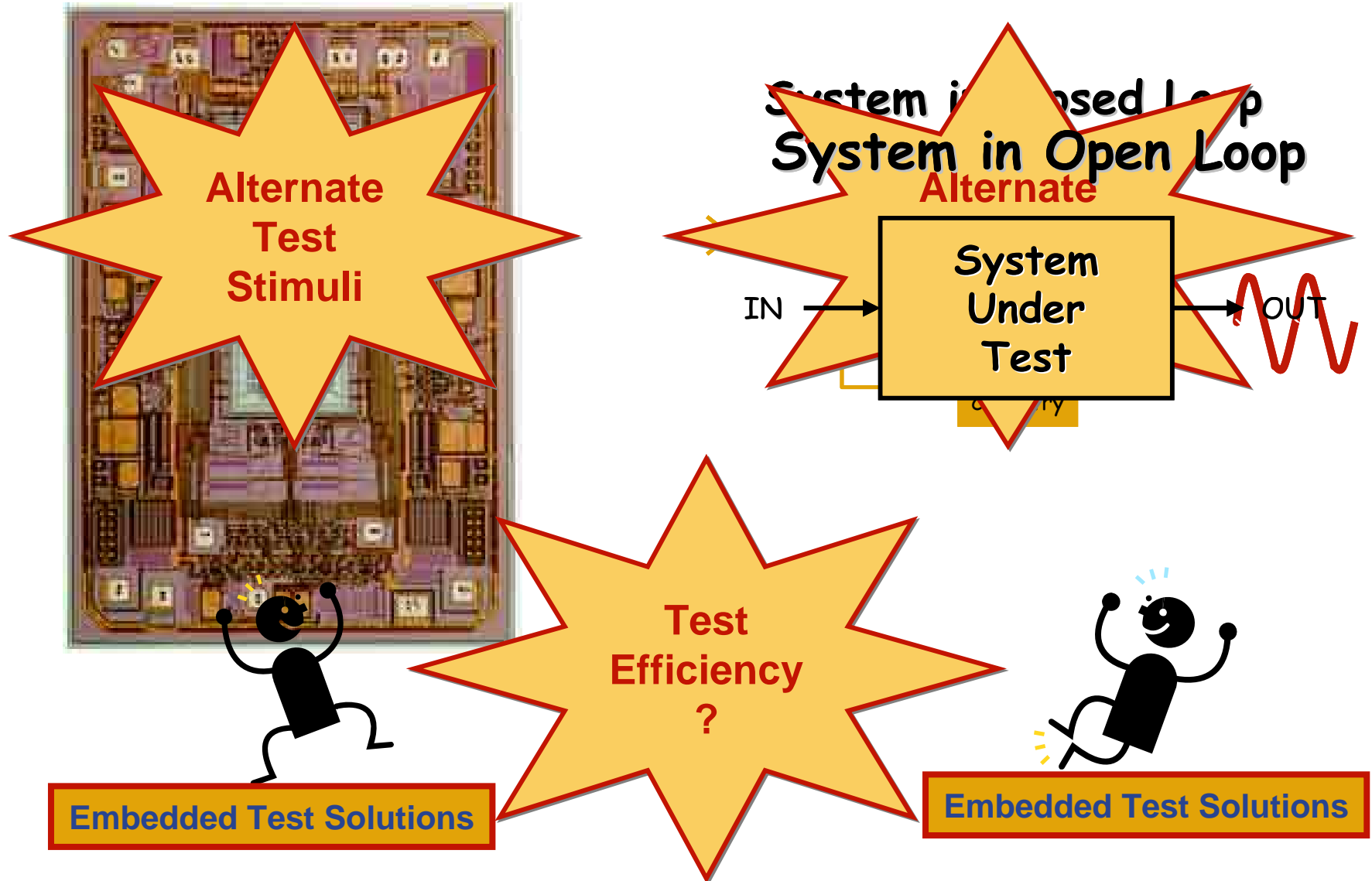
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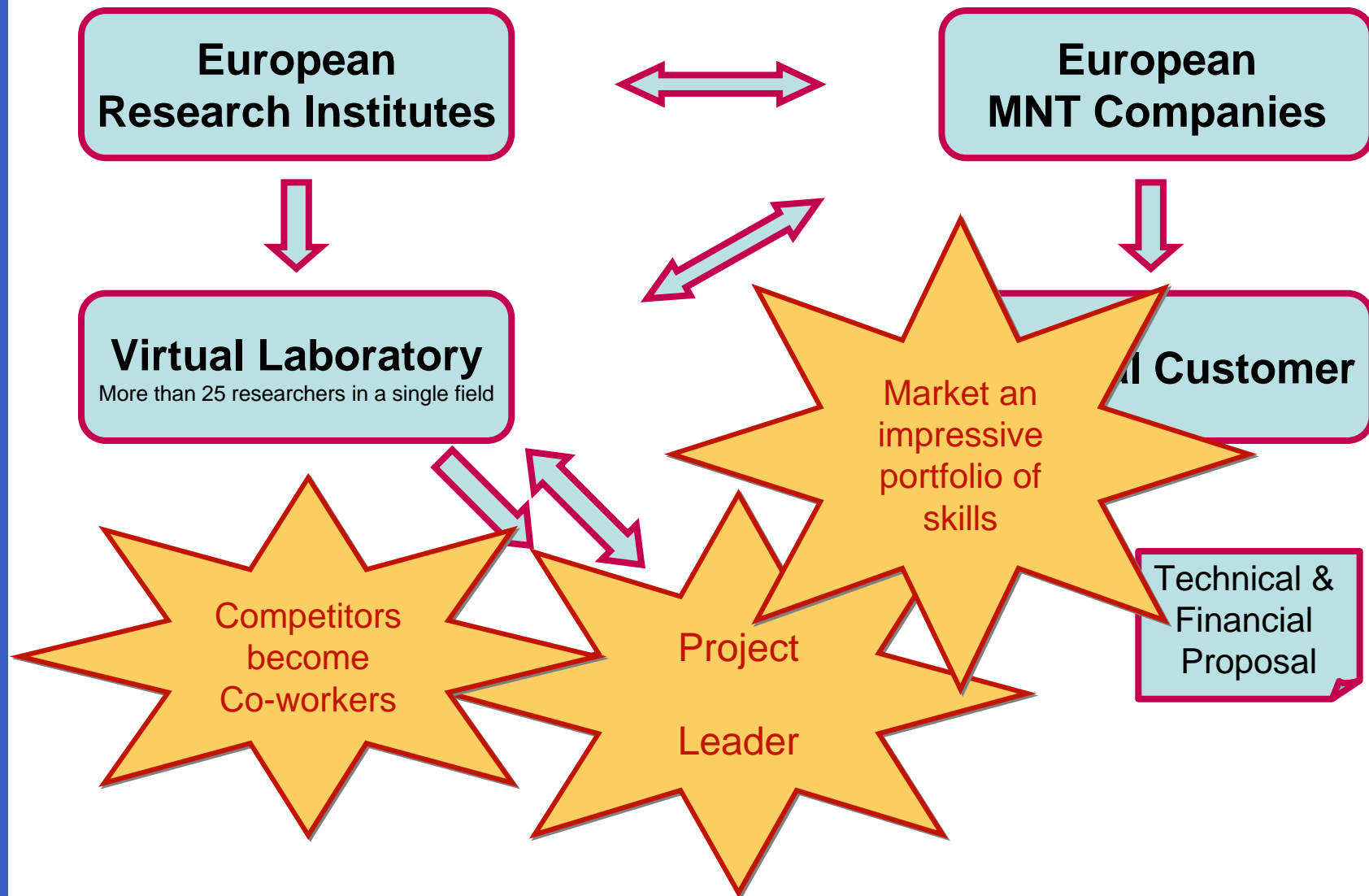
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- Who are we?
 - A virtual laboratory with 25 researchers among the most skilled in Europe
 - 7 localizations meshing Europe
- Why working with us?
 - Close links with other Patent Service Clusters
 - An impressive portfolio of skills
 - Bias superposition, DfT for BioMEMS, Motionless testing of accelerometers, Fault modeling, ...
 - Fault modeling, fault simulation, ...

- A valuable partner for your mass production
 - One stop shop: you're accessing the skills of the entire network through a single interface: 'your' project leader!
 - The project leader define with you the content and negotiate directly with the more skilled partners to define a budget
 - A single contract with the project leader institution or any of the partners
 - More reactive than a single university, the project will be conducted where skills and manpower are available



□ Miscellaneous

- Database of DfT solutions: 100 papers to be extended to 150 in 2007
- Need for harmonization in design flow to include testability: fault model, fault simulation, fault coverage, ...
- FP7 ?