

Reliable Micro and Nano System Design Using Multi Level Process Verification

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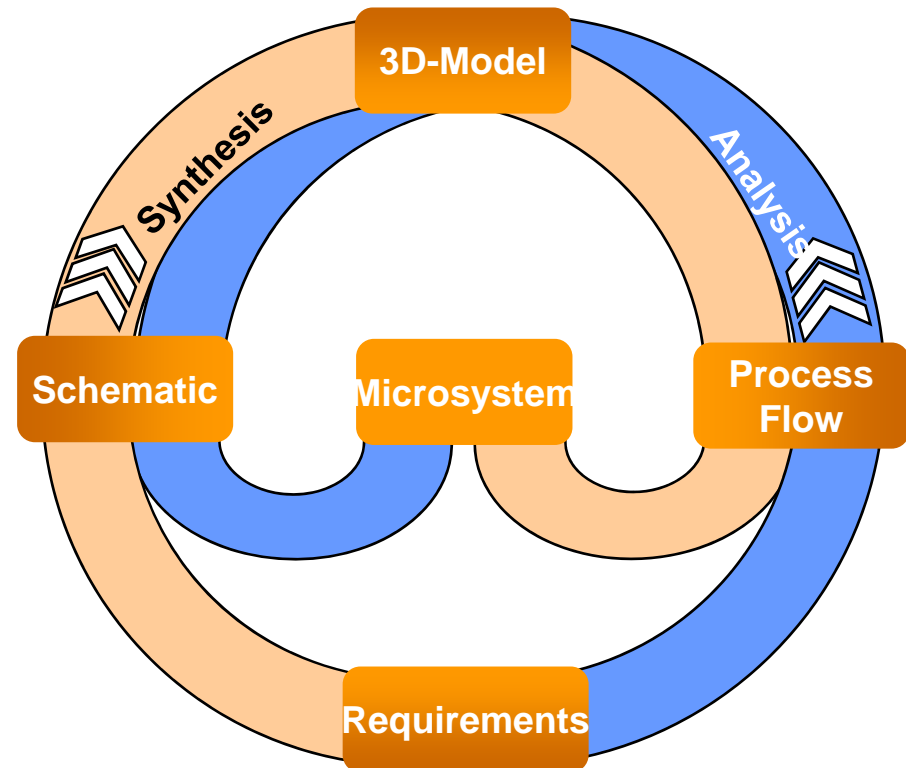


Outline

- **Processes and Reliability**
- **Process Design Flow**
- **Levels of Process Verification**
- **Process Verification Environment**
- **Conclusions**



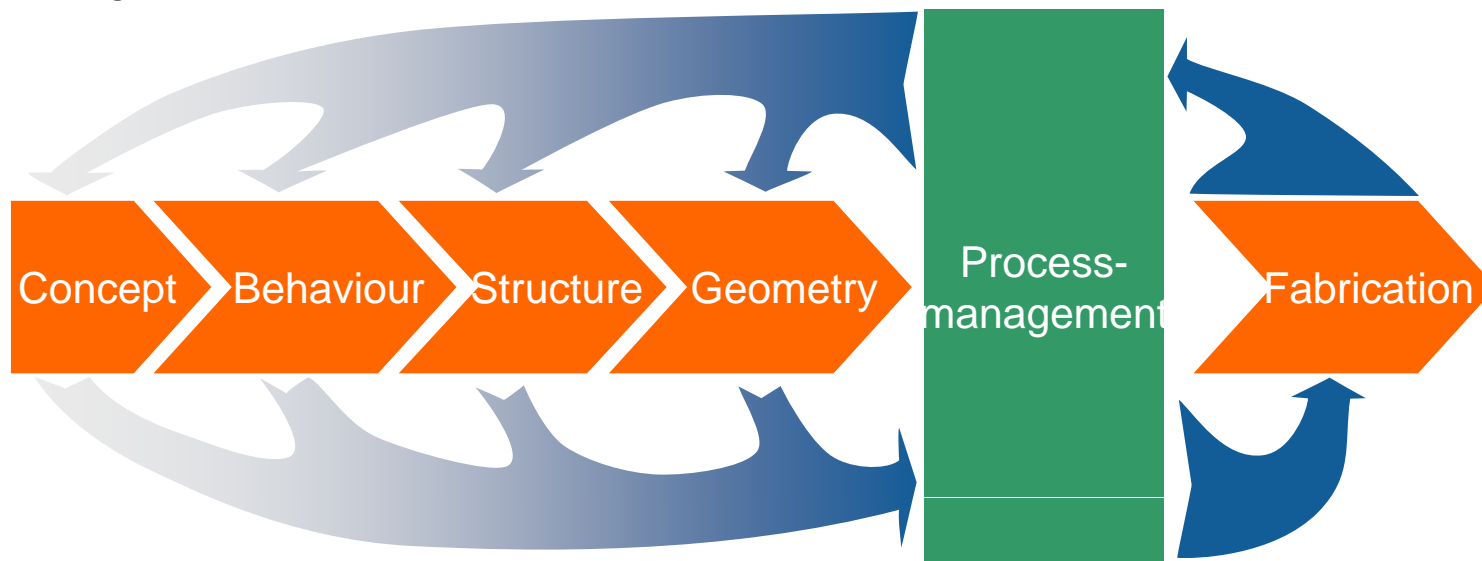
- **Generic design flow for micro and nano systems**
 - Top-down behavioral design
 - Synthesizing a schematic representation and a 3d model of the intended micro/nano structure from a given set of requirements defining
 - *the intended functionality*
 - *all constraints from the intended application environment*
 - Bottom-up fabrication-oriented design
 - Creating a process flow matching the 3d model and assuring
 - *manufacturability*
 - *compliance with the intended fab machinery*
 - *optimum yield*
 - Top-down and bottom-up flows are strongly interwoven





- **Design flows and reliability**

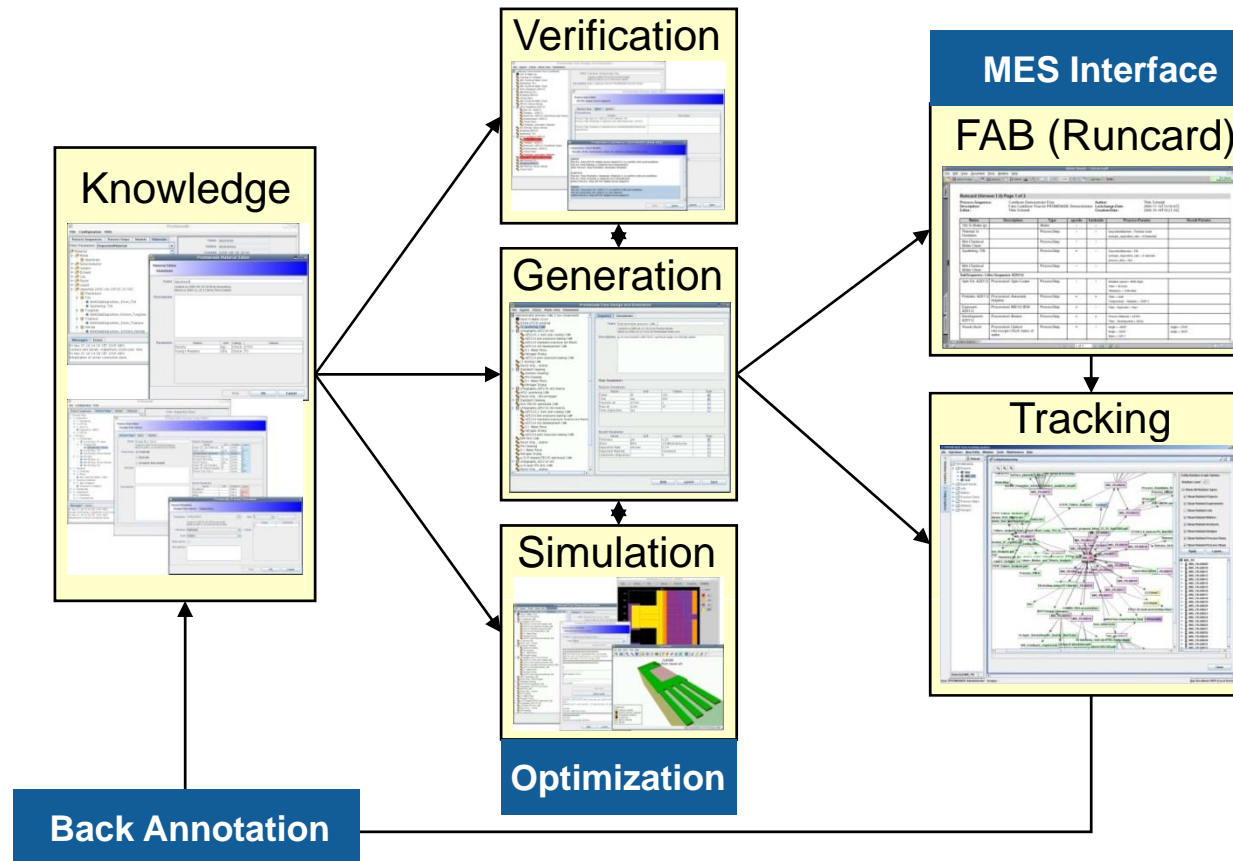
- In micro/nano system design all design stages are strongly influenced by process knowledge
- Reliable system design requires reliable process design!
 - on all levels of abstraction
 - in a continuously increasing level of process definition detail
 - with acceptable additional effort (design time) for process flow generation and verification





Process Design Flow

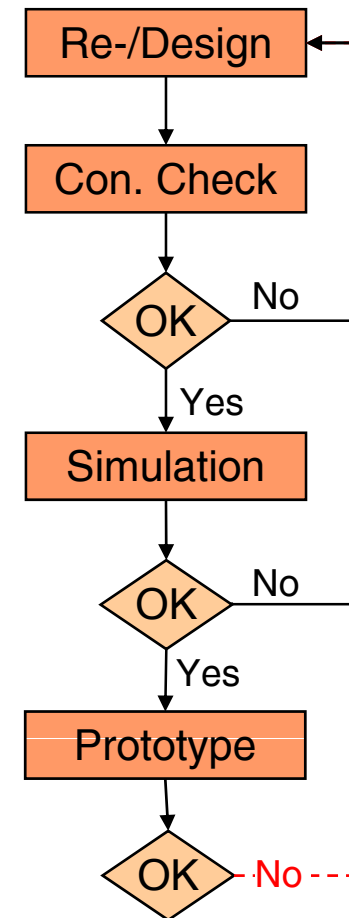
- **Reliable process management makes use of**
 - a comprehensive process knowledge base
 - process optimization with multi-level verification capabilities
 - intelligent interfacing of process design and fab environment





Stages of Process Flow Verification

- **Consistency checking**
 - to ensure manufacturability and feasibility
- **Process simulation**
 - to allows the assessment of device structures and functionality
- **Experimental verification**
 - to validate process flows in production environment





Stages of Process Verification

- **LEVEL 1: Consistency Checking**
 - Requirements
 - A knowledge-base of process steps, materials, process step parameters, effects, etc.
 - A process flow editor allowing the construction of process flows and configuration of parameters from process related objects in the knowledge base
 - Verification step
 - Checking compatibility rules associated with the process related objects used to construct the process flow
 - Verification result
 - Assessment of the principle viability of the assembled process flow

Qualitative process flow viability assessment



Stages of Process Verification

• LEVEL 1: Consistency Checking

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Promenade Process Sequence Editor
IMEC DEMONSTRATOR SIMULATION RUN1

Export Check Mask-Sets Simulation

IMEC DEMONSTRATOR SIMULATION RUN1 (cutlong: ...)

- BASIC WAFER
- Basic Clean
- 50nm Thermal Oxide
- 300nm LPCVD nitride
- Resist spinning-recipe1
- Pre-bake
- OCTEST-mask1 (L#1)
- Basic develop
- Post-bake
- Dry etch LPCVD nitride with stop on thermal oxide
- Basic strip
- 15nm Titanium
- 10nm Titanium Nitride
- 600 nm Tungsten
- CMP of CVD Tungsten with stop on LPCVD nitride
- 1000nm PECVD Nitride
- Sinter 450 30min
- Resist spinning-recipe1
- Pre-bake
- OCTEST-mask2 (L#2)
- Basic develop
- Post-bake
- Dry etch PECVD nitride with stop on tungsten
- Basic strip
- 1600nm PECVD Oxide
- CMP of PECVD oxide with stop on PECVD nitride
- sinter 450 1h
- 100nm poly-SiGe
- Resist spinning-recipe1
- OCTEST-mask3 (L#3)
- Basic develop
- Dry etch poly-SiGe with stop on PECVD oxide and PECVD nitride
- Basic strip
- Wet etch HF:IPA

Promenade Consistency Check Results (Read only)

Consistency Check Results
Results of the consistency check of IMEC DEMONSTRATOR SIMULATION RUN1

ERROR:
Process-Step Dry etch poly-SiGe with stop on PECVD oxide and PECVD nitride is in conflict with postcondition:
Process Step Post-bake is required once immediately after Process-Step Basic develop

ERROR:
Process-Step Resist spinning-recipe1 is in conflict with precondition:
Process Step Pre-bake is required once immediately before Process-Step OCTEST-mask3 (L#3)

WARNING:
Process-Step CMP of PECVD oxide with stop on PECVD nitride is in conflict with precondition:
Process Step DRY ETCH is required once immediately before Process-Step sinter 450 1h

WARNING:
Process-Step 1000nm PECVD Nitride is in conflict with precondition:
Process Step DRY ETCH is required once immediately before Process-Step Sinter 450 30min

Help Close



Stages of Process Verification

- **LEVEL 2: Process simulation**
 - Requirements
 - A knowledge-base containing simulation models assigned to all process-related entities, esp. process steps
 - An interface to process step and device simulators
 - A simulation setup and driver engine
 - Verification step
 - Performing complete process flow simulations by selecting appropriate simulations models and setting up sequences of simulator calls
 - Verification result
 - Simulated 3d-visualization of the effects of executing the process flow

Quantitative process flow viability assessment



Stages of Process Verification

- **LEVEL 2: Process simulation**

- Requirements

- Verification

- Validation

The screenshot shows the Promenade Flow Design and Simulation software interface. The main window displays a 2D layout of a cell with various layers (L#1 to L#4) and a 3D model of the structure. A 'Promenade Process flow simulation' dialog box is open, showing the simulation tool 'Clever', the step name '# Step no 59 "Freeze Release CAM"', and the status 'finished'. The dialog also shows the result files 'save.str'.

appropriate

flow



Stages of Process Verification

- **LEVEL 3: Experimental verification**
 - Requirements
 - Access to real-fab data for process parameter values and distributions
 - Fast concurrent simulation capabilities
 - Verification Step
 - Setting up an experimentation tree and performing process flow simulations with varying process step settings
 - Verification Result
 - Process parameter settings that assure manufacturability with best possible results

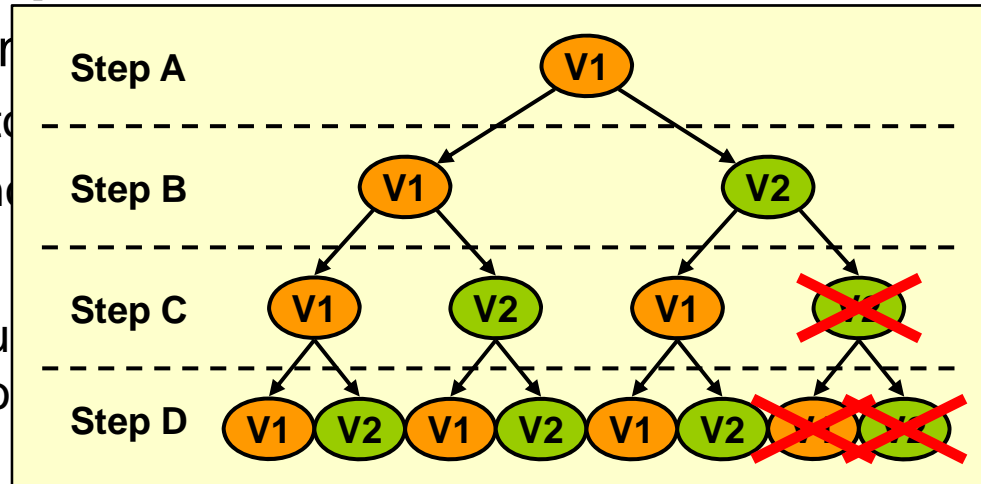
Real-life (fab-data-related) process flow viability assessment



Stages of Process Verification

● LEVEL 3: Experimental verification

- Requirement
 - Access to
 - Fast con
- Verification
 - Setting u
 - simulation
- Verification



and distributions

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Promenade Flow Design and Simulation

Promenade Process Simulation DOE Tree

File Export Check Mask-Sets Simulation Help

DOE of Demonstrator process CAM_2

4 Si Wafer (110)

Si3N4 LPCVD external

Cr sputtering CAM

BHF Etch CAM

Freeze Release CAM

BHF Etch CAM

Freeze Release CAM

Cr sputtering CAM

BHF Etch CAM

Freeze Release CAM

BHF Etch CAM

Freeze Release CAM

Si3N4 LPCVD external

BHF Etch CAM

Freeze Release CAM

BHF Etch CAM

Freeze Release CAM

Info Status

Name Cr sputtering CAM

Status finished

Input Deck

Step no 22 "Nitrogen Drying"

this step is neglected in the simulation

Step no 23 "AZ5214 post exposure baking CAM"

this step is neglected in the simulation

Step no 24 "HfO2 sputtering CAM"

rate.depo machine=24 material="Hafnium_Oxide" cvd step.cov=0. dep.rate=1

u.s

deposit machine=24 time=0.05 seconds divisions=7

#deposit material="Hafnium_Oxide" thickness=0.05 divisions=7

Step no 25 "Resist strip - Microstripper"

Simulation Output

PCTHERDOS

ATHENA> # Step no 32 "AZ5214 pre exposure baking CAM"

ATHENA> # this step is neglected in the simulation

ATHENA>

ATHENA> # Step no 33 "AZ5214 standard exposure reverse"

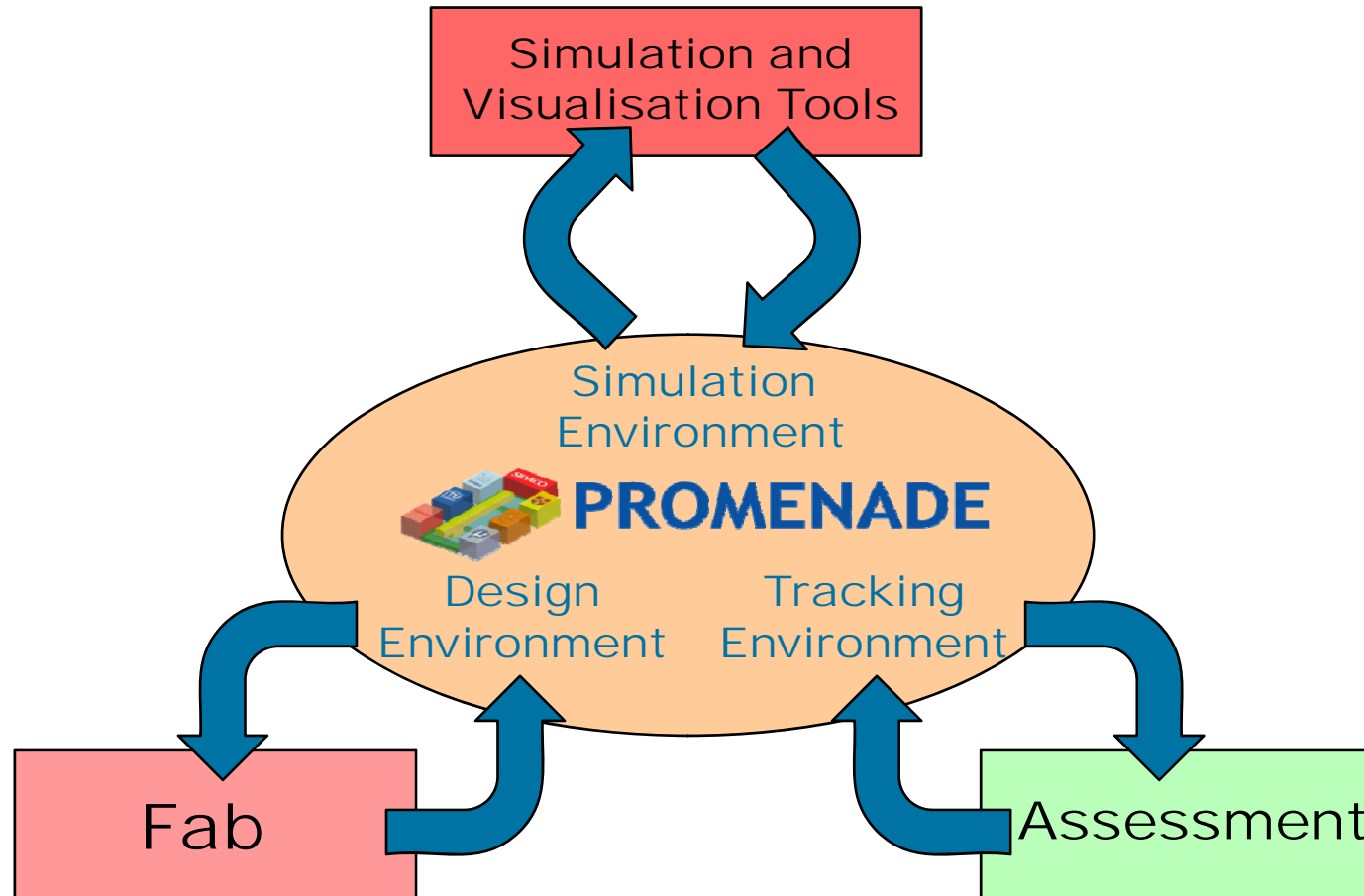


Process Verification Environment

- Process design and tracking



PROMENADE



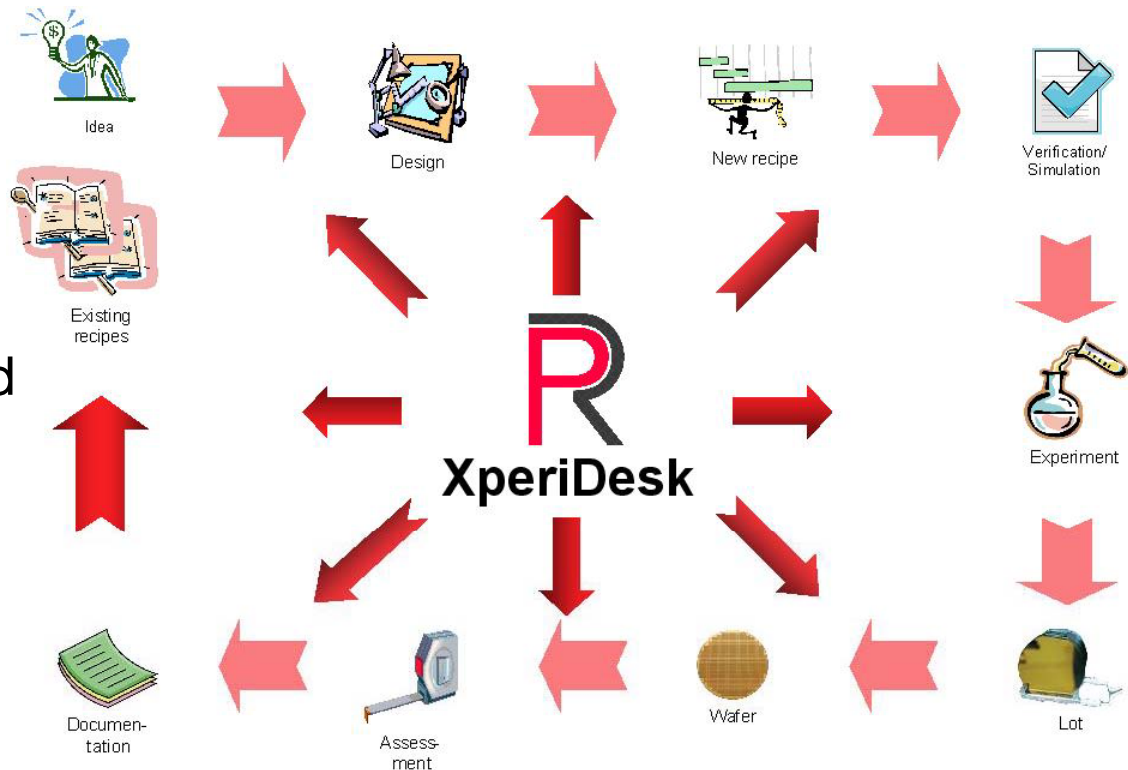
Developed in EU-FP6-project IST-1-507965



Process Verification Environment

● XperiDesk

- Complete round-trip support for process management flow
- Supporting experiment based development and optimization of silicon thin film manufacturing sequences
- Process design and verification
- Interfacing simulation and MES
- Complete document management and intra-project communication capabilities



Process Relations

Put structure into the 'art' of Process Development



Process Relations GmbH, Emil-Figge-Str. 76-80, D-44227 Dortmund
www.process-relations.com
info@process-relations.com



Conclusions

- **Reliable micro/nano systems require reliable fabrication processes**
- **Reliable process design can be assisted by process management and design tools covering**
 - High-level process verification by consistency checking of abstract process flow models
 - Medium-level process verification by extended process flow simulations
 - Low-level process verification by active experimentation
- **Tool support available: XperiDesk (PROMENADE)**
- **Future research topics**
 - Integrating bottom-up (process design) and top down (behavioral) flows and design frameworks
 - Supporting concurrent, integrated design of mask layout and process flow
 - Providing tools for knowledge-based fab data exploration