





2nd Technology Roadmapping Event
on Packaging of MEMS

08 June 2006

Location: Fraunhofer IZM (Berlin)

	<i>Institutes</i>	<i>Authors</i>
	Heriot-Watt University	Fabien Holler
	QinetiQ Ltd	Alan Brown
	Fraunhofer Institute for Reliability and Microintegration (IZM)	Olaf Wittler
	4M2C	Patric Salomon

What is Patent-DfMM?

An EU-funded Network of Excellence, which aims to provide European industry with support in the field of "Design for Micro and Nano Manufacture (DfMM)". The Network is organised around 7 Work Packages including "Packaging" and "Business Development".

Workshop objectives

- As a result of the first workshop at Heriot-Watt University, a list of Packaging "*High-Level Challenges and Related Issues*" was produced (see appendix 1). During the day, the participants will work on 4 of these High-Level Challenges. They will:
 - ↳ Prioritise these related issues, and
 - ↳ Identify key developments / R&D projects to address them

Following a questionnaire exercise, it was decided that the 4 High-Level Challenges that will be tackled are:

- ↳ Low-cost Wafer Level Packaging and related testing techniques
 - ↳ Improvements in CAD/Modelling
 - ↳ Hermetic/vacuum packaging and low-cost alternatives (near hermetic, plastic packages...)
 - ↳ Improved reliability
- This will enable the selection of packaging investment opportunities, not just for the short term needs of Patent-DfMM, but also for industrialists and academics in the long term. Topics that will be identified as "highly relevant and strategic" for European industry will also be brought into the relevant EC consultation efforts and stakeholder activities such as NEXUS.
 - The workshop will therefore contribute towards industrial take-up of MEMS, the enhancement of Patent-DfMM capabilities, and future EC strategies.

What you will gain out of the day

- Advanced knowledge of the latest packaging trends in MEMS
- An opportunity to network with academics and industrialists active in MEMS packaging
- The final roadmap report
- A chance to influence decision makers in MEMS and the EC through the Patent-DfMM Network of Excellence

Agenda

Timing	Activity
9.30 – 10.00	Reception and registration
10.00 – 10.30	<i>Fabien Holler, Heriot-Watt university</i> - Introduction - Summary of findings after 1 st workshop: High-Level Challenges and Related Issues - Objectives for the day
10.30 – 11.30	<i>1st brainstorming activity: LOW-COST WAFER-LEVEL PACKAGING (and related testing techniques)</i> Based on the results of the first workshop, participants will expand and rank the Related Issues for low-cost WLP. They will then identify a succession/time line of key developments / R&D projects to address selected issues of the highest priority.
11.30 – 12.30	<i>2nd brainstorming activity: IMPROVEMENTS IN CAD/MODELLING</i> Other High-Level Challenges will be tackled in the same way during the following brainstorming sessions.
12.30 – 13.30	LUNCH
13.30 – 14.30	<i>3rd brainstorming activity: HERMETIC/VACUUM PACKAGING AND LOW-COST ALTERNATIVES</i>
14.30 – 15.30	<i>4th brainstorming activity: IMPROVED RELIABILITY</i>
15.30 – 15.45	BREAK
15.45 – 16.15	<i>Facilitated discussion</i>
16.15	Wrap-up session and depart

Contact

To register or for more details please contact Fabien Holler (f.holler@hw.ac.uk, +44 (0)131 451 4300) or Dr. Olaf Wittler (olaf.wittler@izm.fraunhofer.de, +49 (0)30 464 03 247), or fill in the registration form.

Directions

Fraunhofer IZM, Berlin
Gustav-Meyer-Allee 25
Geb. 17.2

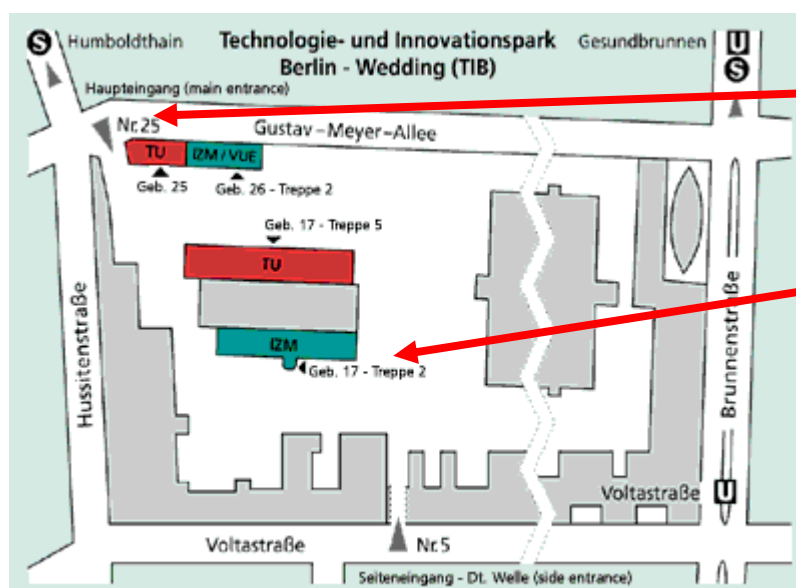
Phone:
+49 (0)30 / 46403-100



By Car From A 115 (Avus) motorway onto A 100 (Stadtring) in northerly direction following signs for Wedding the Stadtring becomes Seestraße, then turn right into Müllerstraße, this continues as Chausseestraße, then left into Liesenstraße, which becomes first Scheringstraße, then Gustav-Meyer-Allee.

By Rail From Berlin-Zoo station, take U 9 underground to the Osloer Strasse terminus, and change to the U 8 (in the direction of Hermannstraße) as far as Voltastraße, then on foot to the Institute.

By Air From Berlin-Tegel airport, take bus no. 128 to Osloer Strasse, then as above. Alternatively you can take a taxi (approx. 20 min)



Main entrance

Geb. 17 – Treppe 2
Visitors entrance via 4th floor

Appendix 1: Selected information extracted from outcomes of the first workshop

The full list of High-Level Challenges and Related Issues will be given to all participants on the day.

High Level Challenges and related issues	Term (S/M/L)	Priority (L/M/H)
Hermetic/vacuum packaging and low-cost alternatives (near hermetic, plastic packages...)		
Clarification of definitions (what is hermeticity, vacuum, low cost?)	S	H
OUTGASSING: - Impact of outgassing / post assembly performance issues - Type of outgassing and impact on MEMS - Control of outgassing (getter on "cold" surfaces, and again: device and application dependent)	M	M
What level of hermeticity is needed (mbar V-1 s-1) (1) at manufacture and (2) during product lifetime (device dependent/application dependent). How to decide ideal rate for near hermetic packages?	M	H
How to characterise hermeticity (M/C-STD)? Definitions of safety margin for reasonable life time and setting up of standards for hermetic/near-hermetic packaging	S	H
Information gathering on how to use getters to improve / control vacuum. In particular: impact of getters and sealing materials: compromise performance/cost	S	H
Patterning capabilities for getters (deposition of materials): getters are conductive, so reducing size creates need for better patterning to use available area efficient. For instance, shadow masking will not be sufficient anymore when reducing the size for RF switches below 1x1mm total area of CSP	S	H
Getters: temperature of activation affecting MEMS	M	L
Materials selection for capping wafers, sealing materials (application dependent, e.g. space, bio-medical, transmissive packaging media...)	S	H
Electrical/optical interface and impact on hermeticity	M	M
Improved organic low surface energy coating (teflon like, parylene, insulating thermoplastic coatings...)	S	H
Low-cost Wafer Level Packaging		
Low cost = high vol, automation issues	M	H
Yield optimisation, quality	L	H
Cavity atmosphere and control	M	M
Assessment techniques: suitable wafer level testing	S	H
Commercial access to WLP, especially vacuum	M	M
Develop interposer technology to match MEMS device to low cost packaging options (not exclusive to WLP technologies)	S	H
Thermal characterisation of WLP packages	M	H
Properties of sealing materials (polymers etc)	M	M
CMOS compatibility of WLP. Sealing and interconnect process. To provide hermetic package on CMOS with SMT compatible layout you need a convenient solderable metallization on CMOS, provided by the CMOS foundry.	S	H
Improvements in CAD/Modelling		
Package co-design (mixed model device). But standard packages are an underlying issue	M	H
Accurate modelling and estimation of accelerations factors of new evolving MEMS package technologies: analysis and predictions of life time, material degradation, fatigue and fracture of packaging materials under harsh environments (moisture, Temperature...)	L	H
Development of reduced order modelling for packaging for device-package interaction	S	H
Improved multi-physics linked models: thermal electrostatic, optical, electronic, surface performance over temperature, deformation, etc...	M	M
Material parameters & CAD, e.g. bulk / thin film	M	M
Accurate modelling and estimation of accelerations factors of new evolving MEMS package technologies: improved analysis and modelling of the behaviour of material interfaces (diffusion, moisture, and delamination)	L	H