

Manufacturing Starts with the Design

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"Manufacturing starts with the design" - this statement holds especially true in the case of micro- and nanosystem technology. The commercialisation of Microsystem Technology is still severely limited despite a range of impressive research programmes, design innovations and initiatives across Europe. Some of the key problems that affect manufacturability are now widely acknowledged and include the development of economic engineering and production test programmes and packaging influences. Improved design support is also becoming a key commercial requirement with pressure on tool vendors to optimise models aimed at providing the designer with the means to predict the impact of second-order effects on the design (e.g. package induced stress and mode coupling), and verify end-use stability and subsequent reliability, especially in aggressive environments (high temp / temperature gradients, vibration, electromagnetic radiation). The need to solve these issues in microsystem technologies is hampered by the shortage of multidisciplinary, skilled engineers, the immaturity of the "Electronic Design Automation (EDA)" environment and the lack of tools to build closed loop models that run efficiently in hierarchical, multi-domain simulation environments. Furthermore, many typical applications of micro & nano system technologies require very high reliability, and suitable test methodology, standards and instrumentation are often missing. Time-to-market targets for most Microsystem products will therefore only be achieved if these so called "back-end" issues are addressed early in the design cycle.

Today, it is widely acknowledged that Microsystems Design is not optimised for mass production due to the immaturity of design environments, support tools and design methodologies. Furthermore, packaging frequently causes serious tech-

nical problems in microsystem products: The package should form a cheap but reliable interface between the active device and an often harsh, demanding environment. The device to package interaction, nowadays mostly neglected during design, tends to be more severe than in electronics-only devices. In addition, test and reliability verification have become a severe bottleneck, as they must verify complex behaviours rapidly, at low cost and with minimum access across multi-domain interfaces. These combined issues have been a dominating factor in the failure of many microsystem applications to move from prototype

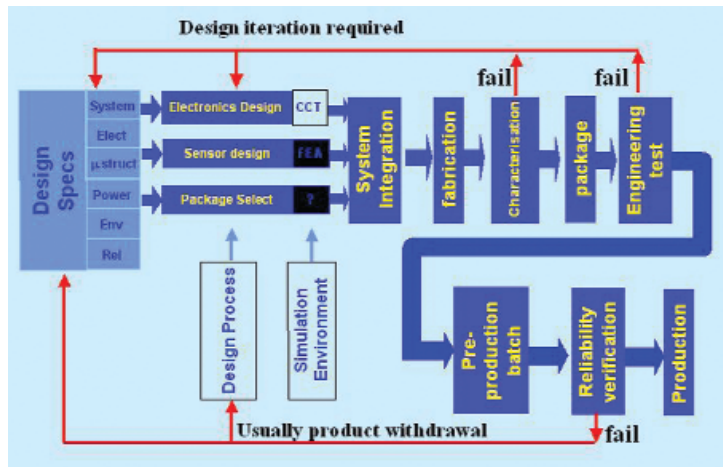


Figure 1: The Current Design and Manufacture Cycle for Microsystems

to pre- & full production, due to excessive design and manufacture costs or doubts about end-use reliability.

The design process described in fig.1 for the system functional units - electronic design, sensor design, package selection - is decoupled mainly due to the lack of appropriate design and simulation tools and know-how. Decisions regarding package solutions tend to be intuitive. Although some "Finite Element Modelling (FEM)" of

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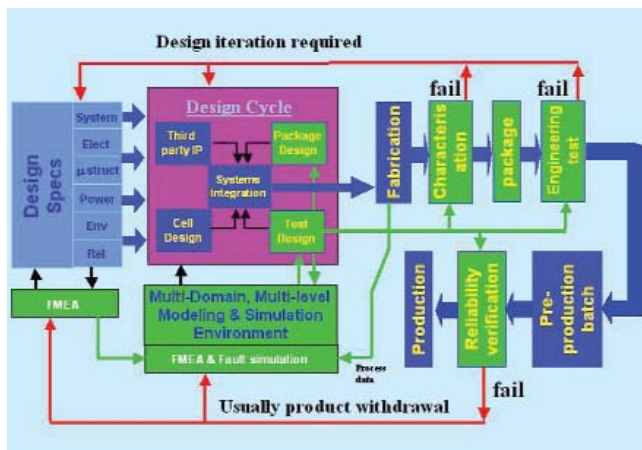


Figure 2: Target Design & Manufacture Methodology

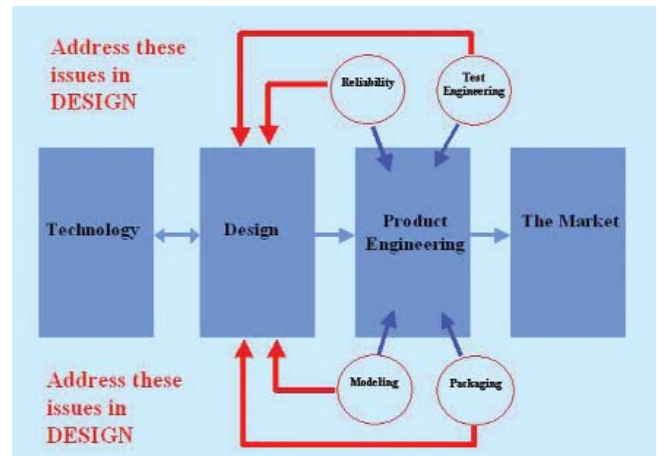


Figure 3 Manufacturing Issues to be addressed in the Design Phase

package options is carried out, the norm is to employ 'experience'. A similar situation exists in the context of test, which is mostly perceived as a post design task. This design and manufacture cycle often results in major difficulties in guaranteeing specifications across full operating conditions and, in most cases, pushes tests cost to above 50% of total manufacturing costs.

As a result of all these problems, several design iterations are required for post prototype manufacturing. It is clear that in order to reduce the number of redesign cycles, "design for manufacture" activities have to be moved from the back-end into the front-end design cycle. All activities needing action are identified in green in figure 1. The way this could be achieved is illustrated in figure 2. This includes working closely with designers to initiate a "Failure Mode and Effect Analysis (FMEA)" programme at the specification stage. This FMEA has to ensure robustness and testability as well as environmental tolerance. All of these issues have to be adequately addressed during each single design phase. Design challenges such as the integration of test support functions, auto compensation for non-linearity and offset drift mechanisms are essential elements that have to be taken into account by "design for manufacture" procedures. Note that the approach presented in figure 2 requires a fully integrated simulation environment to ensure that for example the package induced effects of temperature cycling on the microsystem design at anchor points can be predicted or the ability of a cut-off frequency or

gain measurement to detect a critical parametric failure mode can be assessed. Fortunately, considerable progress in behavioural simulation environments has been made through for example the standardisation of the IEEE VHDL-AMS language, which allows complex interactions between physical systems and analogue as well as digital electronic variables.

It is clear therefore that technical problems late in the design phase or post prototype fabrication can only be avoided by integrating the ability to model, evaluate and compensate for potential second order effects introduced in manufacture during the front-end design. In addition, reducing the cost of manufacture requires an early analysis of probable failure and degradation modes and, where practical, integration of test support functions to either simplify the test process or self-monitor key parameters on or off-line.

To be successful in integrating manufacturing issues into the design phase, it is required to pull together a critical mass of European experts in packaging, test and reliability engineering. This both to optimise existing back-end techniques and to work with simulation and modelling experts in order to provide designers with the tools that help to avoid test, reliability and package problems. This should lead to an effective "design for manufacture" approach (figure 3). There is a significant "industrial pull" for this activity that covers end-users and manufacturers of microsystems, microfluidic devices (interface to nano-technology) and

MOEMS applications across the aerospace, pharmaceutical, automotive, environmental and IT markets.

All key packaging technologies need to be covered, including zero-level technologies such as wafer scale packaging / assembly and level 1, including vacuum packaging, plastic encapsulation, low-cost optical structures and bio-compatible technologies. This requires input from experts in the underlying processes (e.g. anodic bonding, die bonding, wire bonding, electroplating and micro moulding, etc.). The input from test and reliability experts in stress techniques, micromechanical test & characterisation, production test, electrical parameter test methods, Built-in Self-Test, condition monitoring and associated fault modelling is required and a core modelling and simulation support team needs to be established that includes suppliers and modelling experts.

There have been a number of projects addressing test, reliability and packaging issues for microsystem technologies supported by national and European funding. There has, however, been little interaction between these individual projects and fields. An example of why these areas should be pulled together is best illustrated by an analysis of test engineering research. In this domain, most work has been based around test equipment optimisation, built-in self-test concepts for microsystems and fault simulation. In reality, however, the causes of failure in most devices tend to be dominated by packaging and poorly controlled second-order effects that manifest them-

selves as reliability and yield issues. Furthermore, package design and modelling may well benefit from work done in fault modelling and reliability issues are best addressed within the design process through careful modelling and control of key design parameters (e.g. temperature and drift). An effective network of reliability, test and packaging engineers integrated through modelling and simulation research and tied closely into the design environment

appears to be a sensible route to increasing the applications of micro & nano system technology in the marketplace.

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CAD Simulator for Excimer Laser Micromachined 3D Surfaces

Richard Hume, Pio Iovenitti and Erol Harvey

Microstructuring with excimer lasers provides a unique capability, however, achieving complex textures and specific 3D shapes is difficult because of the lack of computer aided tools to improve the efficiency of the design and fabrication stages. The lack of such tools may even inhibit the process achieving its full potential in terms of the type of structures that can be produced. The development of CAD/CAM/CAE systems for conventional engineering applications has taken place over the last thirty years, and may have even reached maturity, with many well-established

systems available on the market today. The benefits of such systems have been proven and adopted by industry. However, CAD tools for microsystems are relatively new, and only a few integrated systems are available today. While the engineering analysis capability of these systems is increasing, the development of process simulation has been in the most part restricted to chemical fabrication. This article describes an approach to producing 3D solid models of a surface produced by excimer laser micromachining which builds on previous research [1,2].

A CAD visualisation tool to represent a surface machined by an excimer laser has been developed. The simulator was developed for an Exitech Limited Series 8000 to automate part programming and assist users develop novel microstructures. The simulation tool enables users to define step and repeat, linear and circular paths, and mask shape, and then view the 3D machined surface. The tool assists users in developing part programs to achieve the desired machined surface structure and reduces the need to use expensive laser machining time as well as providing an alternative to the trial and error method of part

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